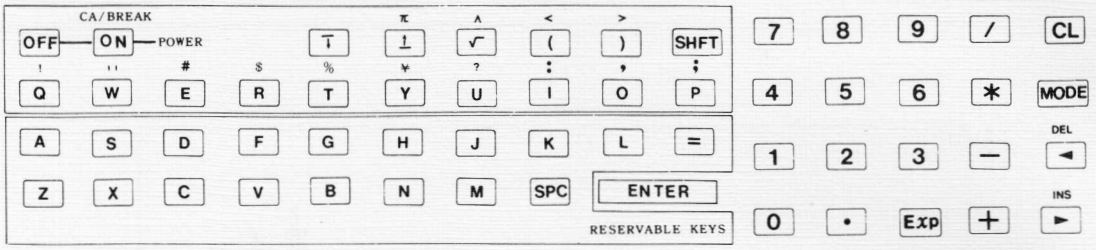
SHARP
SERVICE MANUAL

MODEL PC-1211, CE-121

CONTENTS

SHARP CORPORATION

1. SPECIFICATIONS



1-1. Display

- Display tube: LF8017JE
- Display method: 5 x 7 dot matrix liquid crystal
- Display capacity: 24 coulumns (alphanumerics and symbols)

1-2. Basic functions

- Computational capacity: 12 digits of mantissa and 2 digits of exponent.
- Computational method: According to mathematical formula (with priority consideration and judge function)
- Capacities:
  - Program memory; 1424 steps, max (PC1211)
  - Data memory; Fixed memory
    - 26 memories
    - Flexible memory (commonly usable with the program memory)
      - 178 memories, max (PC1211)
  - Reserve program; 18 kinds, 48 steps, max
  - Input buffer; 80 steps
- Buffers:
  - Data buffer; 8 stages
  - Functional buffer; 16 stages (but 15 stages for parenthesis)
  - Subroutine buffer; 4 stages
  - "FOR NEXT" stagement buffer: 4 stages

1-3. Arithmetic functions

Add (+), Subtract (–), Multiply (+), Divide (/), Power raising (∧)

Trigonometric functions:	SIN (sine), COS (cosine), TAN (tangent)
Inverse trigonometric functions:	ASN ($\sin^{-1}$), ACS ($\cos^{-1}$), ATN ($\tan^{-1}$)
Logarithmic functions:	LOG (common logarithm), LN (natural logarithm [ln])
Exponential functions:	EXP (exponential)
Angular transformations:	DMS (decimal notation to sexagesimal notation), DEG (sexagesimal notation to decimal notation)
Square root extraction:	$\sqrt{\ }$
Signum function.	SGN
Absolute value:	ABS (| X |)
Interization:	INT

Execution of arithmetic operation is commanded by the ENTER key.

1-4. Editorial functions

Cursor shift:	▶ (right), ◀ (left)
Insertion:	INS
Deletion:	DEL
Line control:	↓ (down), ↑ (up)

1-5. Programming language

BASIC (Beginner's All purpose Symbolic Instruction Code)

1-6. Power source

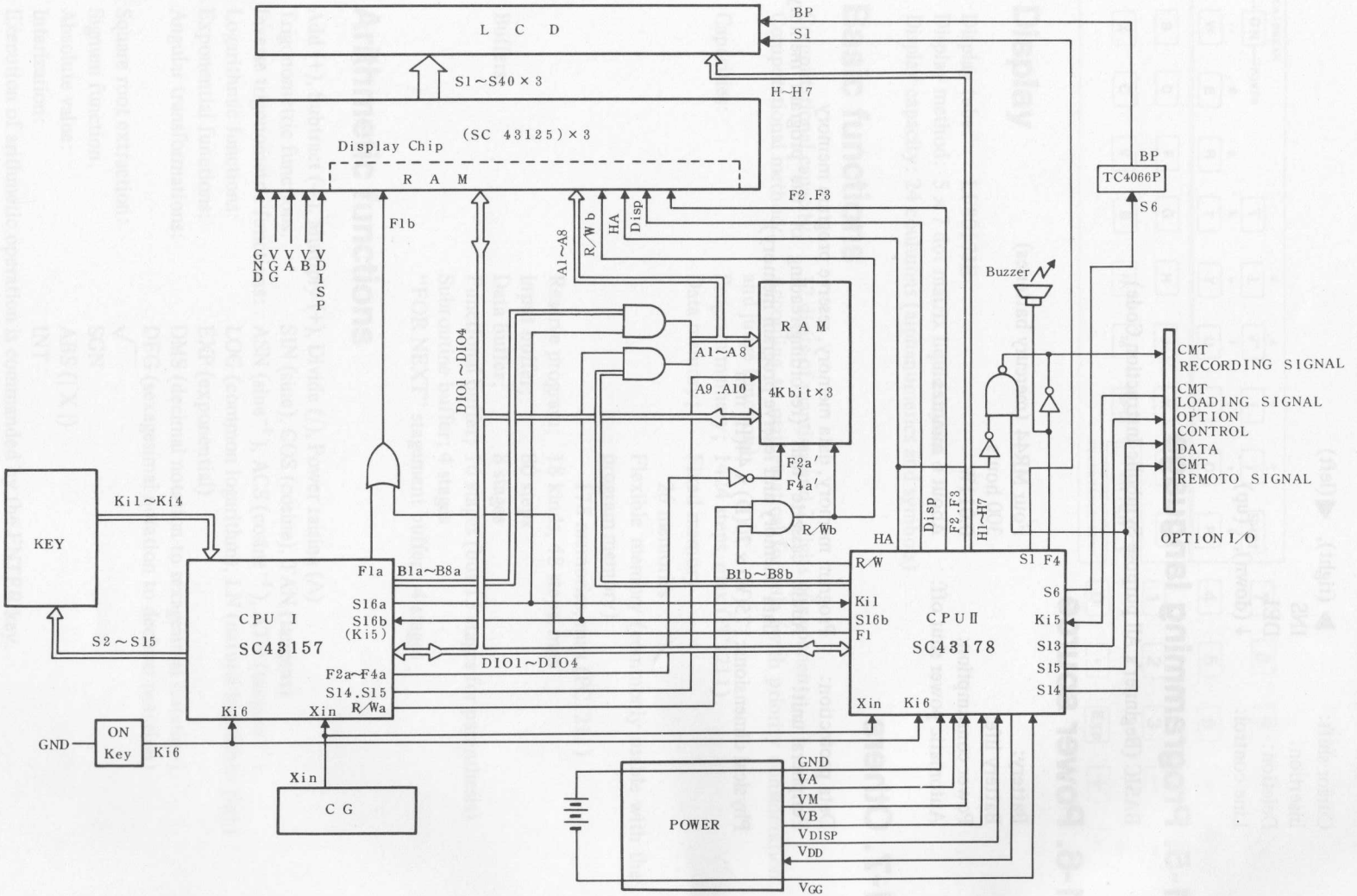
Battery:	Four MR44 (mercury batteries)
Battery life:	300 hours
Power consumption:	0.011W
Automatic power shut off:	About 6 minutes

1-7. Others

Data protection:	Program memory, data memory, reserve program memory
Peripheral unit:	Audio cassette unit (recording/reading of the program memory, data memory and reserve program memory)

Physical dimensions: 175(W) x 70(D) x 44(H) mm

2. BLOCK DIAGRAM



System configuration (see the system block diagram)

System of this unit consists of the following components:

1) CPU I (SC43157) x 1
2) CPU II (SC43178) x 1
3) 4K-bit RAM (TC5514P x 3)
4) Display chip (SC43125 x 3, with built-in RAM)
5) 2AND gate (TC4011UBP x 1)
6) 2AND 2OR (TC4019BP x 1)
7) Inverter (TC4069BP x 1)
8) Quard Analog Switch Multiplexer (TC4066BP)
9) LCD (24-digit FEM dot LCD)
10) Key
11) Crystal (CSB2560)

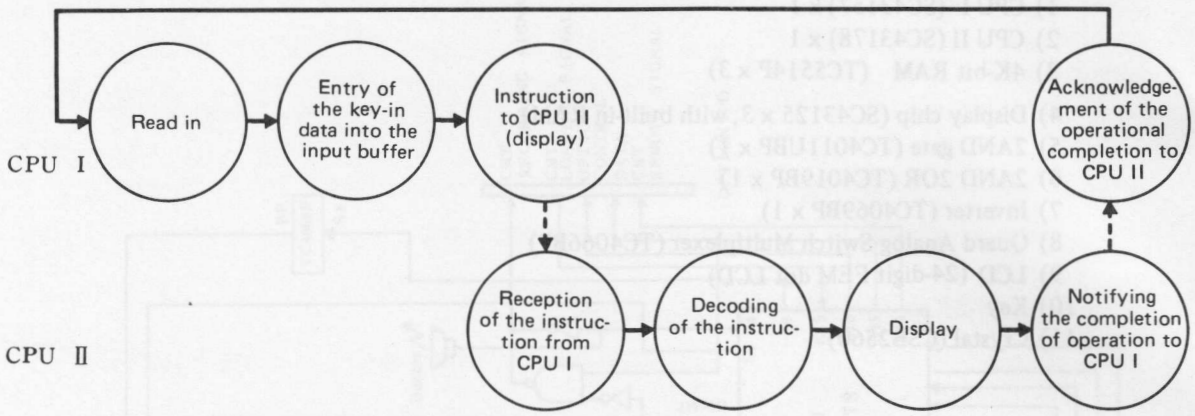
2-1. CPU I, CPU II

These CPUs are provided with internal ROM, and each of CPUs shares the following assignments:

CPU I	CPU II
Key input routine	Display processing routine Input buffer Computational result Error
Acknowledgement of the remaining program	Arithmetic routine
One instruction to one program step incorporation	Character generator
Interpreter: Program execute statement Cassette control statement Command statement Printer control	Cassette routine
	Print routine
	Buzzer
Execution of manual operation	Recognition of printer
Power shut off control	Power off
Clock stop control	Clock stop

- The CPU I functions to read key-in data or read the instruction to be executed from the RAM, and decides what is to be done for the control of arithmetical operation (i.e. control of arithmetic sequence, memorizing of arithmetical data, and its readout), or interprete the syntax of the BASIC instruction for deciding what is to be executed, or determines and prepares the information to be displayed, but the CPU I does not perform any execution by itself. It only arranges the data and information in proper sequence and acts to provide instruction code to the CPU II via the buffer. On the other hand, the CPU II constantly receives execution instructions from the CPU I via the transfer buffer and executes operation against each of instructions or sometimes performs to exchange data depending on the situation. Although it shares major part of execution in term of execution, it performs some kinds of auxiliary CPU when looked in the view that it does not perform any decision by itself.

Ex: Actions of CPU I and CPU II at the time of key data entry.

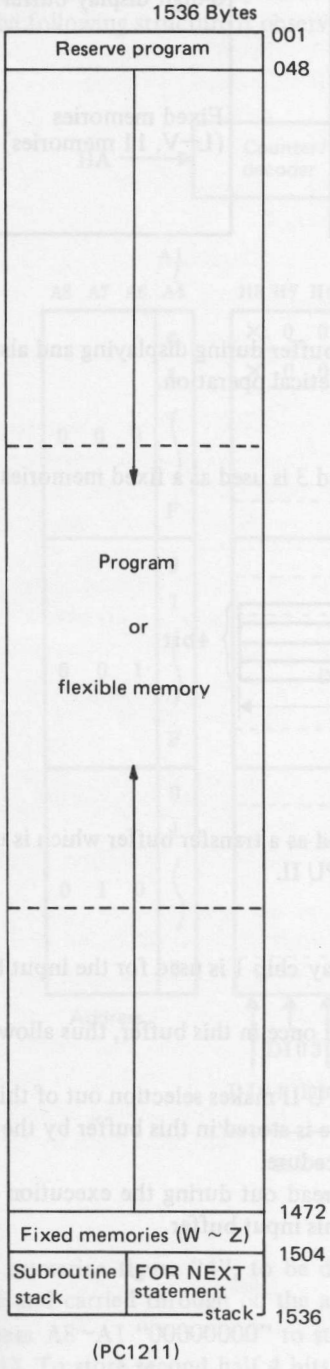


In the case of manual operation of the pocket computer, the instruction code (key code) is written into the RAM in the display chip (input buffer) after information is put through the keyboard and converted into the instruction code by the CPU I, then this instruction code (display, at this case) is transfered to the CPU II via the transfer buffer. As the CPU II receives this instruction, the CPU II then decodes this instruction (display, at this case) and executes display processing. Upon the completion of this processing, it is then notified to the CPU I, then the CPU I confirms the completion of the task by the CPU II before terminating their jobs.

2-2. RAM

A certain number of C-MOS RAM (1 ~ 3 chips, 4K bits each) and another RAM incorporated inside the display chip are used in this pocket computer, having varieties of configurations as described below:

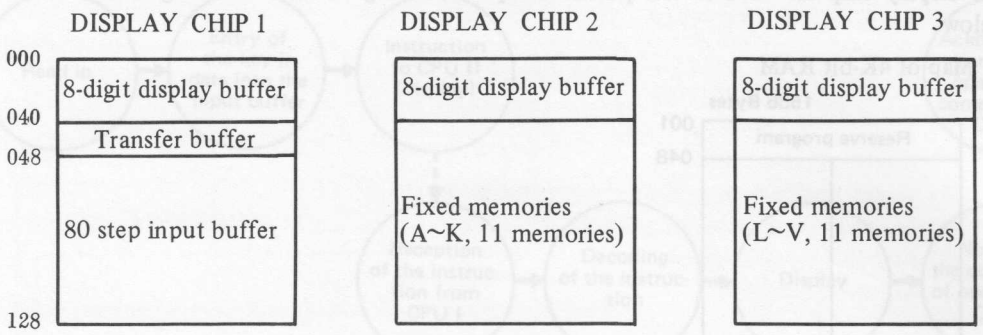
- Map of 4K-bit RAM



(PC1211)

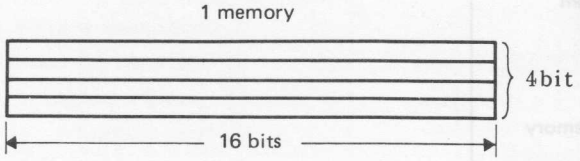
Although RAM area is mainly shared by the program, data and reserve program memories, it is also used for the subroutine stack, FOR NEXT statement stack and fixed memories (W, X, Y, Z).

- Map of the RAM incorporated in the display chip
  There are three 1K-bit RAMs (128 bytes each) incorporated in each of display chips (SC43125), having the following configurations:



- 8-digit display buffer
  40 bytes of 8-digit display buffer is used as a display data buffer during displaying and also used as a buffer memory for arithmetical result during the arithmetical operation.

- Fixed memory
  The total memory of 176 bytes from the display chip 2 and 3 is used as a fixed memories, A~V (22 memories).



- Transfer buffer
  8 bytes (1 memory equivalent) of the display chip 1 is used as a transfer buffer which is used in the transaction of instruction between the CPU I and the CPU II.

- Input buffer
  Remaining 80 bytes (10 memories equivalent) of the display chip 1 is used for the input buffer, which is used in the following functions:
  1. Any information entered through the keyboard is stored once in this buffer, thus allowing up to 80 steps.
  2. The display contents is stored by the CPU I and the CPU II makes selection out of this data.
  3. When an arithmetical instruction is entered, its procedure is stored in this buffer by the CPU I and the CPU II performs operation according to this procedure.
  4. When program or reserve program is to be recorded or read out during the execution of the cassette control instruction, action takes place through this input buffer.

2-3. Display

The contents of display indicated by the CPU I is received by the CPU II via the input buffer and makes converted into respective character codes, then they are carried over to the display buffer in the display chip through the address data bus.

- Designation of the display data
  The following structure is observed in the display buffer in the display chip.

There are 8 x 40=320 bits (40 bytes) of area in the display buffer in the display chip.

Ex: Displaying numerical figure "4"

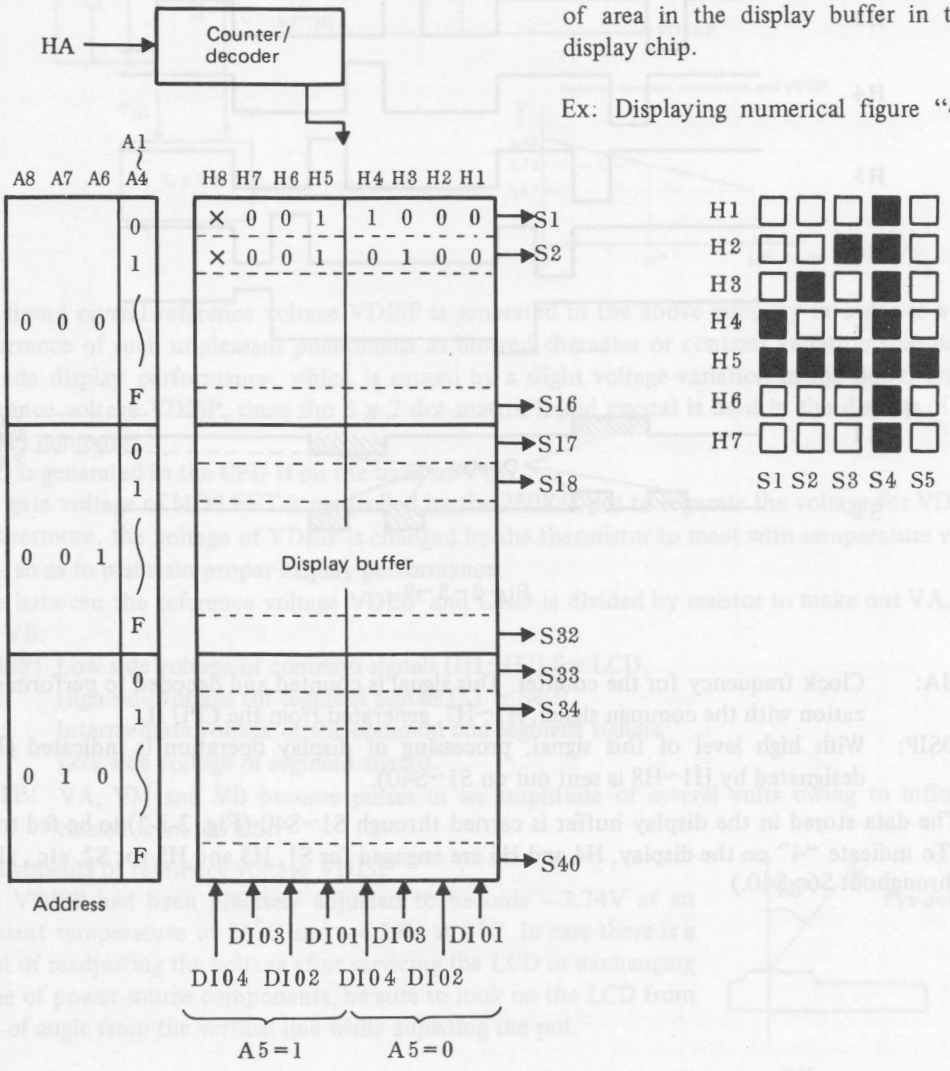


Fig 2-3-1

The numerica figure "4", to be displayed by the CPU II, is converted into the relevant character code and carried through on the address data bus. First of all, the segment S1 is selected with the address A8~A1 "00000000" to store the data DI04~DI01 "1000" in the display buffer (see Fig. 2-3-1). To store second half 4 bits of the data, only A5 in the address in turned "1" to make the address "00010000" to store data "0001". In the same manner, the address "00000001" is selected for storing the first half 4-bit data "0100" for he segment S2 and the second half 4-bit data "0001" is stored with the address "00010001".

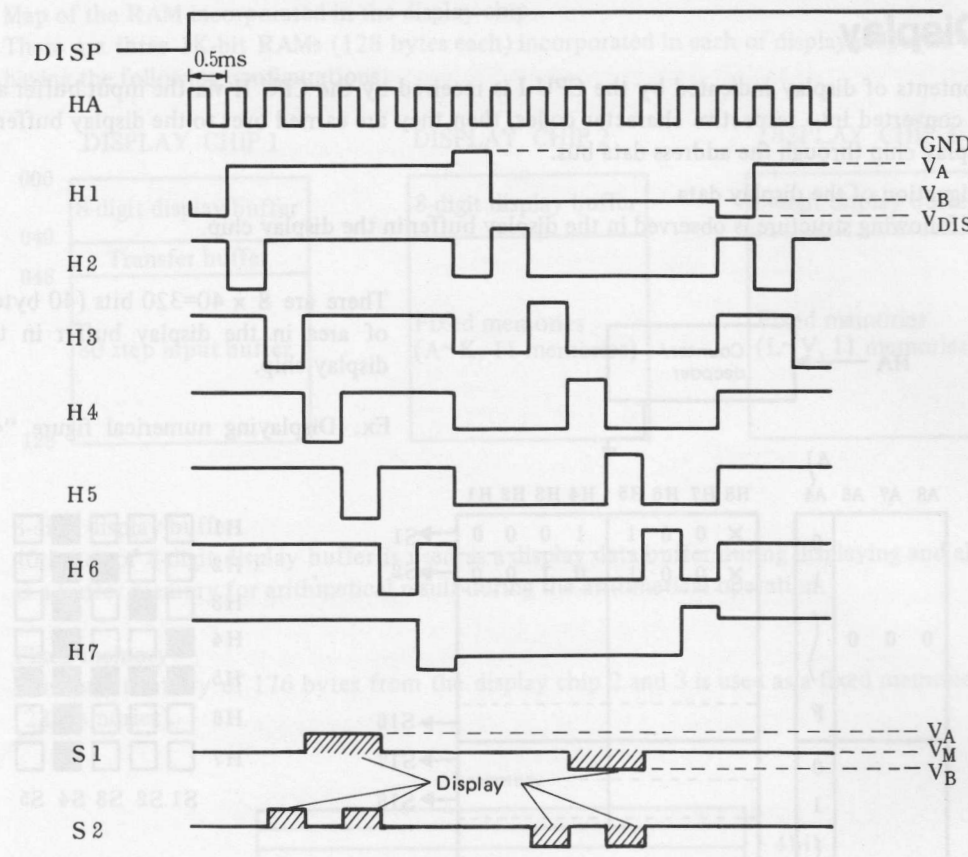


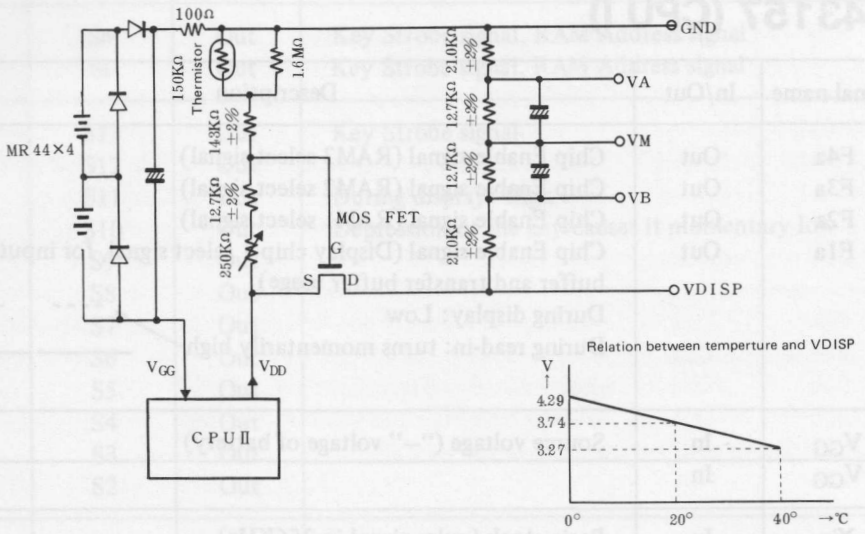
Fig 2-3-2

HA: Clock frequency for the counter. This signal is counted and decoded to perform synchronization with the comman signal, H1~H7, generated from the CPU II.

DSIP: With high level of this signal, processing of display operation is indicated (RAM data designated by H1~H8 is sent out on S1~S40).

The data stored in the display buffer is carried through S1~S40 (Fig. 2-3-2) to be fed to the LCD. (To indicate "4" on the display, H4 and H5 are engaged for S1, H3 and H5 for S2, etc., all the same throughout S6~S40.)

2-4. Power source



○ The liquid crystal reference voltage VDISP is generated in the above circuitry in order to avoid occurrence of such unpleasant phenomena as blurred character or contrast variation that might degrade display performance, which is caused by a slight voltage variation in the liquid crystal reference voltage VDISP, since the 5 x 7 dot matrix liquid crystal is used in the display of this pocket computer.

A) VDD is generated in the CPU II on the basis of VGG.

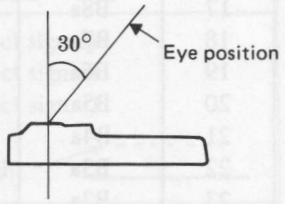
B) The gate voltage of MOS FET is controlled by the 250KΩ pot to regurate the voltage for VDISP. Furthermore, the voltage of VDISP is changed by the thermistor to meet with temperature variation, so as to maintain proper display performance.

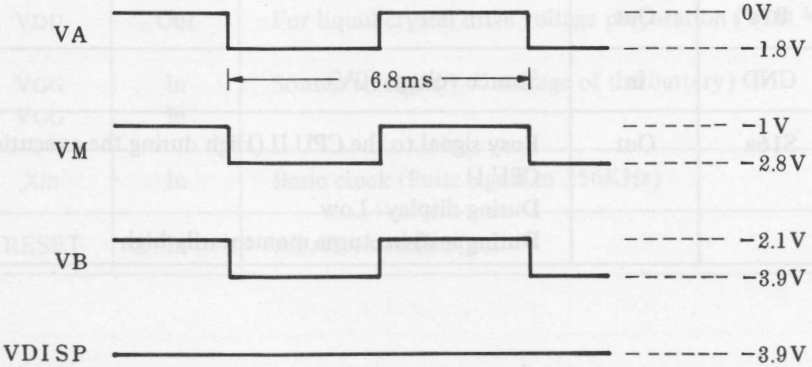
C) Line between the reference voltage VDISP and GND is divided by resistor to make out VA, VM and VB.

VDISP: Low side voltage of common signals (H1~H7) for LCD.
VA: High side voltage for segment signals (S1 ~ S40)
VM: Intermediate voltage of the common and segment signals
VB: Low side voltage of segment signals.
NOTE: VA, VM and VB become pulses in an amplitude of several volts owing to influence caused from the LSI.

○ Adjustments of reference voltage VDISP

The VDISP had been precisely adjusted to become −3.74V at an ambient temperature of 20°C and −4.29V at 0°C. In case there is a need of readjusting the voltage after servicing the LCD or exchanging some of power source components, be sure to look on the LCD from 30° of angle from the vertical line while adjusting the pot.

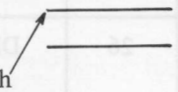




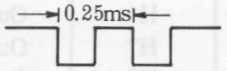
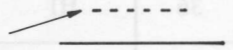
3. LSI SIGNAL DESCRIPTIONS

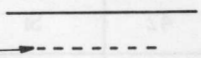
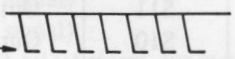
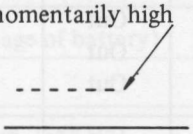
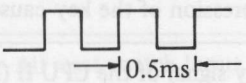
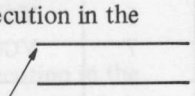
3-1. SC43157 (CPU I)

Pin No.	Signal name	In/Out	Description
1	F4a	Out	Chip Enable signal (RAM3 select signal)
2	F3a	Out	Chip Enable signal (RAM2 select signal)
3	F2a	Out	Chip Enable signal (RAM1 select signal)
4	F1a	Out	Chip Enable signal (Display chip 1 select signal, for input buffer and transfer buffer usage) During display: Low During read-in: turns momentarily high
6	V_{GG}	In	Source voltage ("–" voltage of battery)
7	V_{GG}	In	
8	Xin	In	Basic clock (pulse signal in 256KHz)
9 10	TEST1 TEST2		Connected with GND
11	RESET	In	All reset switch input Normally high but turns low when the all reset switch is depressed.
12	R/Wa	Out	RAM Data Read/Write signal During display: High Depression of the key causes it momentary low.
13 14 15 16	DIO1 DIO2 DIO3 DIO3	In/Out In/Out In/Out In/Out	Data Bus (for address designation of the input buffer and transfer buffer in RAM and display chip 1). During display: High During read-in: Low
17 18 19 20 21 22 23 24	B8a B7a B6a B5a B4a B3a B2a B1a	Out Out Out Out Out Out Out Out	Address Bus (for address designation of the input buffer and transfer buffer in RAM and display chip 1). During display: Mementary generation During read-in:
30	GND	In	Source voltage (0V)
40	S16a	Out	Busy signal to the CPU II (High during the execution in the CPU I) During display: Low During read-in: turns momentarily high

Pin No.	Signal name	In/Out	Description
41	Sn	Out	Key Strobe signal, RAM Address signal
42	Si	Out	Key Strobe signal, RAM Address signal
43	S13	Out	Key Strobe signal
44	S12	Out	
45	S11	Out	During display: High
46	S10	Out	Depression of the key causes it momentary low
47	S9	Out	
48	S8	Out	
49	S7	Out	
50	S6	Out	
51	S5	Out	
52	S4	Out	
53	S3	Out	
54	S2	Out	
55	Ki1	In	Key input signal
56	Ki2	In	
57	Ki3	In	During display: Low
58	Ki4	In	Depression of the key causes it momentary high
59	S16b (Ki5)	In	Busy signal of the CPU II (high during the execution of the CPU II) During display: Low Depression of the key causes it momentary high 

3-2. SC43178 (CPU II)

Pin No.	Signal name	In/Out	Description
1	F4	Out	Buzzer signal When the buzzer is off: Low When the buzzer is on: 
2	F3	Out	Chip Enable signal (Display chip 3 select signal)
3	F2	Out	Chip Enable signal (Display chip 2 select signal)
4	F1	Out	Chip Enable signal (Display chip 1 select signal) During display: Low During read-in: Turns mementarily high 
5	VDD	Out	For liquid crystal drive voltage preparation (VDD ≒ VGG)
6	VGG	In	Source voltage ("–" voltage of the battery)
7	VGG	In	
8	Xin	In	Basic clock (Pulse signal in 256KHz)
11	RESET	In	All reset switch input

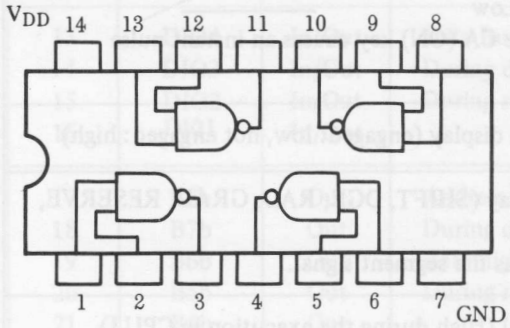
Pin No.	Signal name	In/Out	Description
12	R/W	Out	RAM Data Read/Write signal During display: High During read-in: Turns momentarily low 
13 14 15 16	DIO4 DIO3 DIO2 DI01	In/Out In/Out In/Out In/Out	Data Bus (for data transaction between RAM and display chip) During display: High During read-in: Turns low 
17 18 19 20 21 22 23 24	B8b B7b B6b B5b B4b B3b B2b B1b	Out Out Out Out Out Out Out Out	Address Bus (for address designation of the display chip) During display: B1b=high, B2B=low, B3b=low, B4b=low, B5b=high, B6b=high, B7b=low, B8b=low During read-in: Turns momentarily high 
25	HA	Out	Display signal (Common signal counting pulse) Being generated during displaying 
26	DISP	Out	Display command signal During display: High During execution: Low
27 28 29	VM VA GND	In In In	LCD display voltage (Intermediate voltage of the segment signal) LCD display voltage (High side voltage of the segment signal) Supply voltage (0V)
30 31 32 33 34 35 36	H4 H7 H3 H6 H2 H5 H1	Out Out Out Out Out Out Out	LCD common signals (backplate)
37 38	V_{DISP} V_B	In In	LCD display voltage (Low side voltage of the common signal) LCD display voltage (Low side voltage of the segment signal)
39	S16	Out	Busy signal to the CPU I (High during the execution in the CPU II) During display: Low Depression of key causes it momentarily high. 
40	S15	Out	Record signal to the cassette tape and print data.
41	S14	Out	Remote signal to the MT.

Pin No.	Signal name	In/Out	Description
42	S13	Out	Busy signal to the printer.
43	S12	Out	Expansion signal During display: Low Depression of the CA (ON) key causes an instant pulse generation.
49	S6	Out	For DEF symbol display (engaged: low, not engaged: high)
54	S1	Out	For symbol display (SHIFT, DGE, RAD, GRAD, RESERVE, PRO, RUN) Same waveform as the segment signal.
55	Ki1 (S16a)	In	CPU I Busy signal (High during the execution in CPU I)
56	Ki2	In	Expansion signal To be connected to S12 (CPU II) for PC-1211.
57	Ki3	In	Printer Busy signal Low when the priner is not operated.
58	Ki4	In	Printer connection identifying signal. Low when the printer is not connected.
59	Ki5	In	Cassette reproduct signal.
60	Ki6	In	ON key input signal

3—3 IC

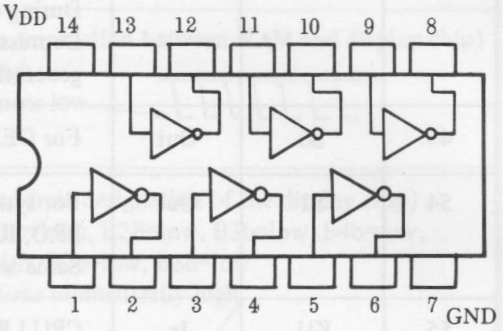
TC4011UBP

(Quad 2-input positive NAND gate)



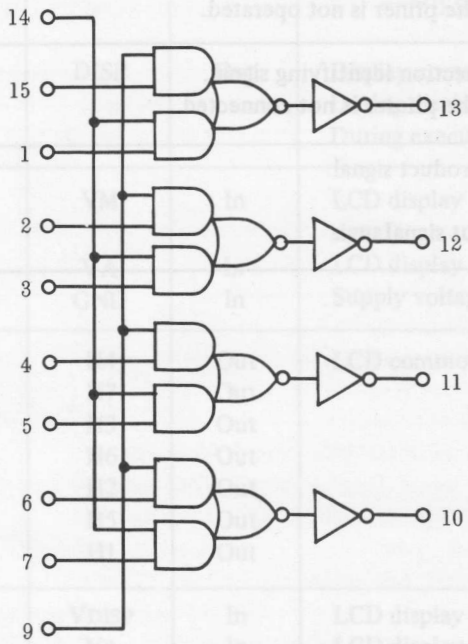
TC4069P

(HEX inverter)



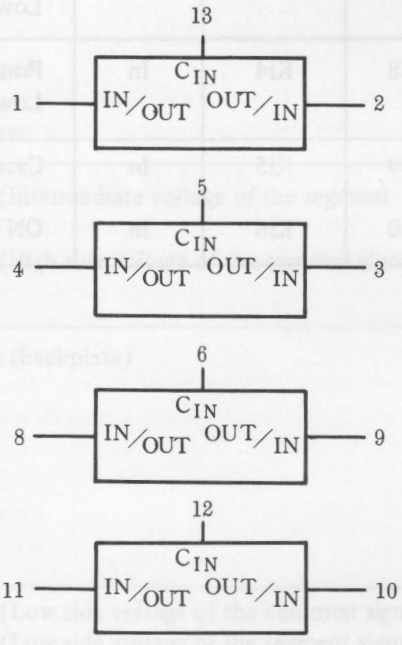
TC4019BP

(Quad AND-OR select gate)



TC4066BP

(Quad bilateral switch)



4. ABOUT SERVICING

- **Disassembly procedure**
  1) Remove the 2 screws (a) and 2 screws (b).
  2) Separate the upper cabinet from the lower cabinet from the screw side, as they are latched together at three points, A, B, and C.

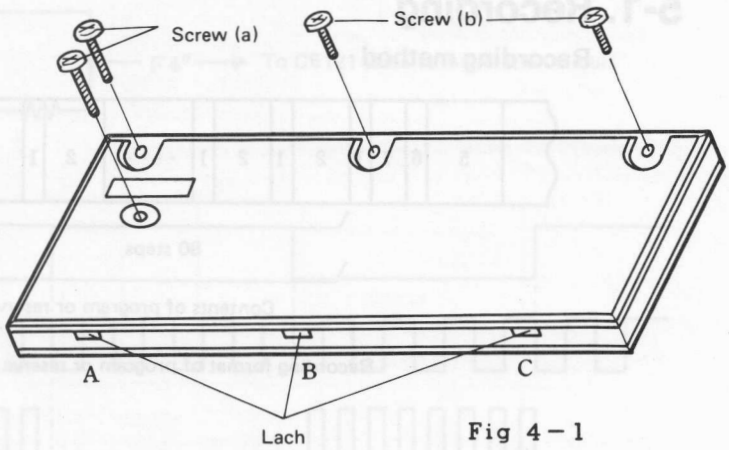


Fig 4 – 1

- **Repairing procedure**
  1) As the back of the arithmetic printed board comes into sight after the removal of the lower cabinet, the arithmetic printed board can be checked from the back side.
  2) Replacement of the CPU II is possible.
  3) If the key printed board is to be checked, the arithmetic printed board has to be bent in right angle after removing the screws (d) and (e). Inspection of the CPU I is possible if the buzzer is removed after removing the screw (c).
  4) The key printed board can be dismounted from the upper cabinet when the 9 screws (f) and 2 screws (g) are removed. But, care must be exercised in dismounting the printed board, as key tops may come falling down one after another.

- **Replacement of the LSI**
  1) It will be much convenient if the LSI use soldering pencil (UKOG-0078CSZZ) is used for replacing the LSI.
  2) Be sure to remove the key printed board from the upper cabinet first, if the LSI on the key printed board is to be removed. If the LSI was removed with the key printed board being fitted on the upper cabinet, there is a possibility of deforming the key rubber by the heat of the soldering pencil.
  3) Be sure to cut the legs of IC, if IC was removed.

- **Measuring current consumption**

Power source voltage. 4.72V
Current consumption:
After depress the ON key: Under 850μA
After depress the OFF key: Under 12μA

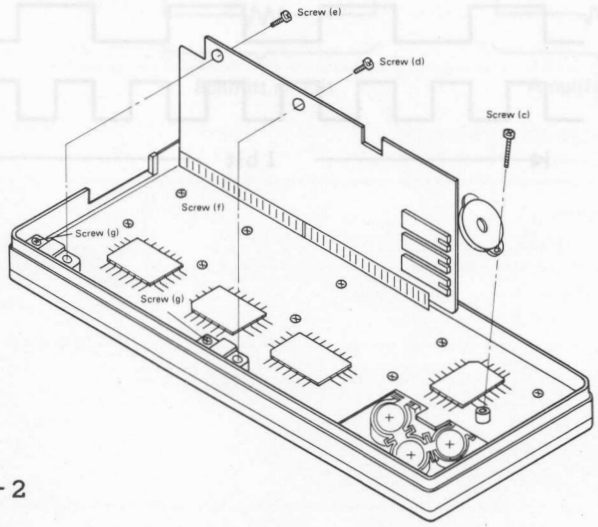
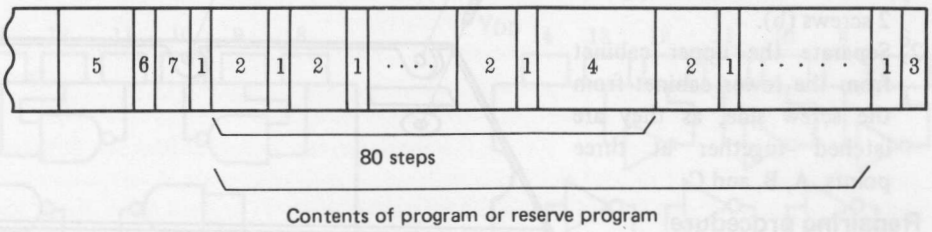


Fig 4 – 2

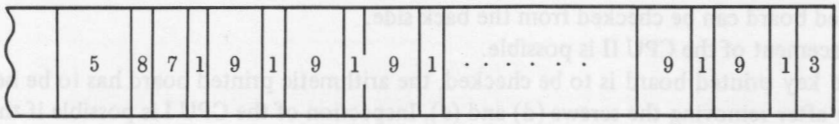
5. CASSETTE OPERATION

5-1. Recording

Recording method



Recording format of program or reserve program

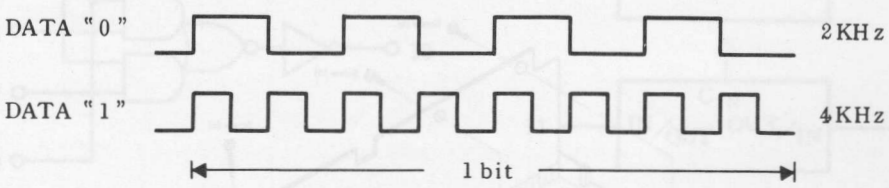


Data memory recording format

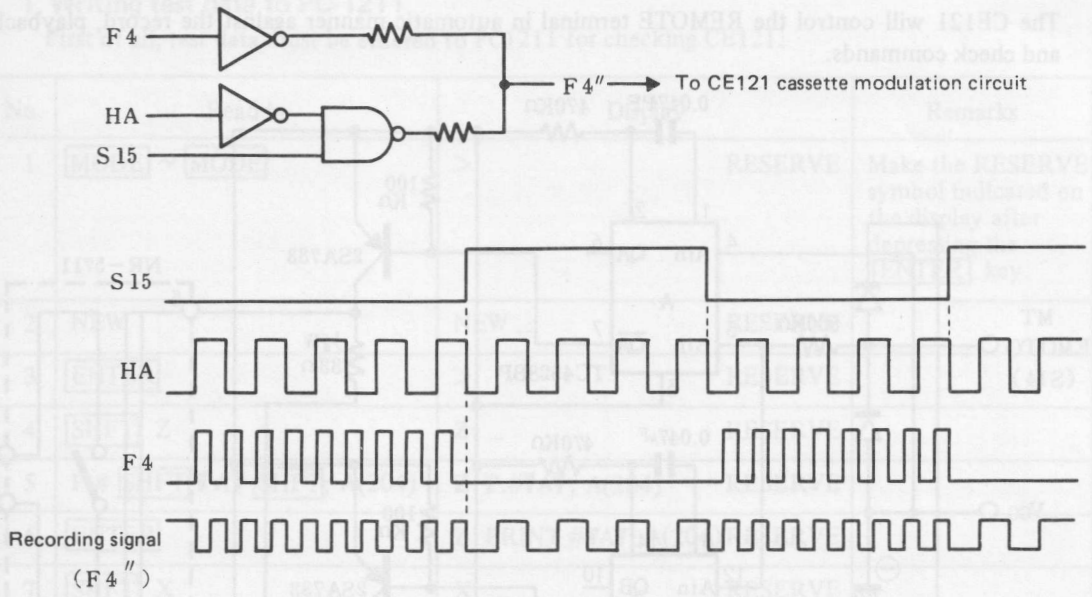
1 = Check sun code (after every 8 steps or one data memory.)
2 = 8 steps of program or reserve program
3 = End code of recording.
4 = This gap, composed of all "1", is inserted at each step the recording exceeds 80 steps, during which teime the next 80 steps of data to be input is prepared in the input buffer.
5 = All "1" is recorded for a period of about 6 seconds in order to avoid non-recordable area located at the top of the tape and is also used for the cueing of the recording head.
6 = With this program or reserve program name is indicated.
7 = File name
8 = Data memory is indicated with this code.
9 = Area for one data memory.

Recording method

Data "0" and "1" are identified by changing the frequency of the recording signal (F4").



Recording signal (F4") generation circuit

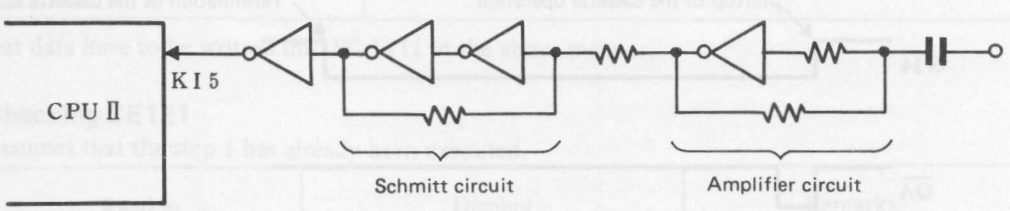


Signal waveform at the time of recording

When recording signal "1" is to be recorded, S15 is turned low level and the signal F4 (clock pulse of ≅ 4KHz) is output during that period. When recording signal "0" is to be recorded, S15 is turned high level and the F4 output is inhibited during that period, at which duration the reverse signal of HA (clock pulse of ≅ 2KHz) is carried on the recording signal.
Then, this signal is supplied to the MIC terminal of the tape recorder via the modulation circuit of the CE121.

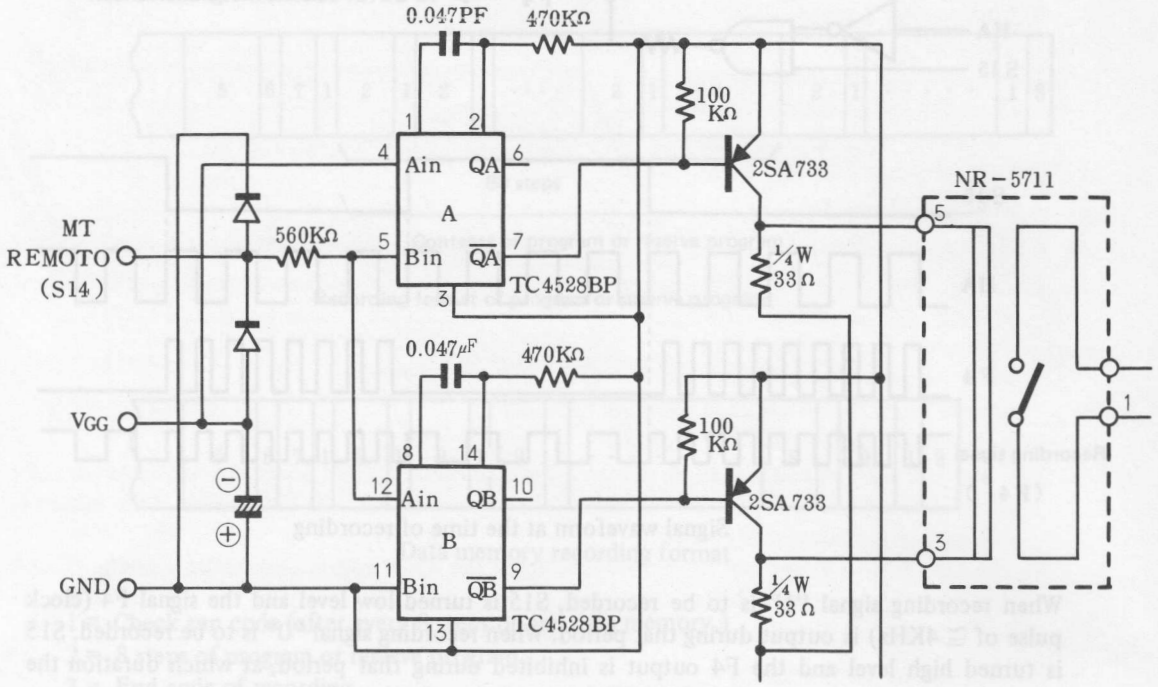
5-2. Reproduction

Output signal from the EAR PHONE jack of the tape recorder is amplified and shaped in the Schmitt circuit, to be input to the CPU II through the Ki5 terminal of the CPU II.



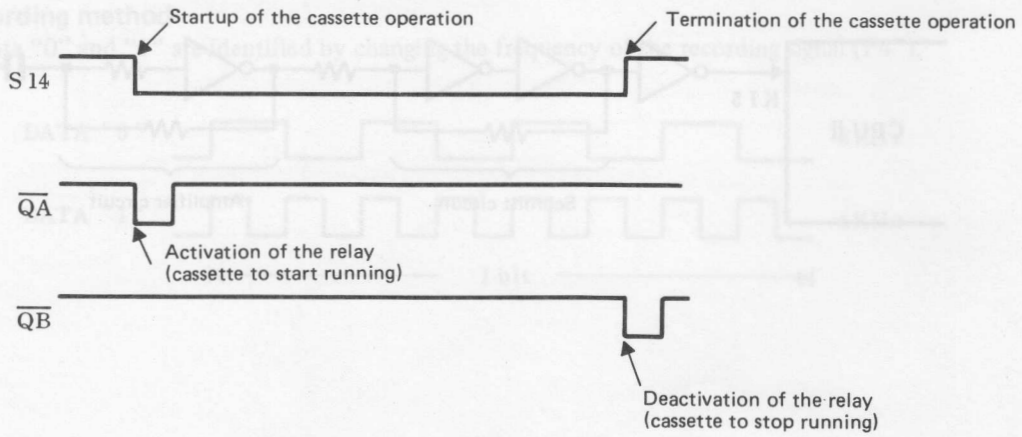
5-3. Remote control

The CE121 will control the REMOTE terminal in automatic manner against the record, playback and check commands.



The TC 4528P is a mono-stable multivibrator which can perform trigger operation and reset operation and two circuits are contained in the same chip.

"A" outputs a pulse which is dependable on the time constant of CR at the falling edge of the input signal, and "B" outputs a pulse which is dependable on the time constant of CR at the rising edge of the input signal. The relay operates ON and OFF according to the current flow to the coil, and it is activated when "A" is active and deactivated when "B" is active.



5-4. Testing the CE121

1. Writing test data to PC-1211

First of all, test data must be entered to PC1211 for checking CE121.

No.	Read in	Display	Remarks
1	[MODE] ~ [MODE]	> RESERVE	Make the RESERVE symbol indicated on the display after depressing the [ENTER] key.
2	NEW	NEW _ RESERVE	
3	[ENTER]	> RESERVE	
4	[SHFT] Z	Z: _ RESERVE	
5	P.# [SHFT] ▼A▼ [SHFT]; A(204)	Z: P.#▼A▼; A(204) RESERVE	
6	[ENTER]	Z: PRINT #▼A▼; A(204) RESERVE	
7	[SHFT] X	X: _ RESERVE	
8	I.# [SHFT] ▼A▼ [SHFT] ; A(76)	X: I. #▼A▼; A(204)_ RESERVE	
9	[ENTER]	X: INPUT #▼A▼; A(204) RESERVE	
10	[SHFT] [SPC]	: _ RESERVE	
11	A(76)	: A(204) RESERVE	
12	[ENTER]	: A(204)	
13	[MODE]	> DEF	
14	[MODE]	> RUN	
15	[SHFT] [SPC] =100	A(204)=100_ RUN	
16	[ENTER]	RUN 100	

The test data have to be written into PC-1211 in the above manner.

2. Checking CE121

Assumes that the step 1 has already been executed.

No.	Read in	Display	Remarks
1	[OFF]		
2			Connect the CE121 with the tape recorder.
3			Connect the PC1211 with the CE121.
4	[ON]	> RUN	Make sure that the symbol RUN is on the display. Otherwise, let the symbol RUN be displayed using the [MODE] key.

No.	Read in	Display	Remarks
5		> RUN	Make sureof the tape recording location.
6		> RUN	Depress the [REC] and [PLAY] buttons. Then, the cassette will come to halt.
7	SHFT Z	PRINT #▼A▼; A(204)_ RUN	
8	ENTER	RUN	The cassette starts to run generating sound.
9		> RUN	The cassette comes to stop quitting sound generation.
10		> RUN	Depress the (PLAY) button. But, the cassette is still at halt.
11		> RUN	Return the cassette tape until the beginning of the recording.
12	SHFT X	INPUT #▼A▼; A(204)_ RUN	
13	ENTER	RUN	The cassette starts to run generating reproducing sound.
14		> RUN	The cassette comes to stop quitting sound generation.
15	SHFT SPC	A(204)_ RUN	
16	ENTER	RUN 100.	
17		RUN 100.	Push the [STOP] button.
18	OFF		
19			Disconnect PC1211 from CE121.
20			Disconnect CE121 from the cassette recorder unit.

I. It requires inspection if one of following conditions is recognized.
   1. When the cassette starts to run at Step 6.
   2. When the cassette fails to run or no sound is heard at Step 8.
   3. When the cassette does not stop at Step 9.
   4. When reproducing sound is not heard at Step 13.

II. Repeat the procedure in the following case.
   1. When "5 ... ..." is displayed at Step 13, repeat operation from Step 10. If the same indication is still on the display, repeat the procedure from Step 5 after entering "A(204)=100". If the same indication is to remain on the display even after this, it requires detailed inspection.
   2. When "100." is not displayed at Step 16, repeat operation from Step 10. If the specific indication does not appear on the display, repeat the procedure from Step 5 after entering "A(204)=100". If the specific indication is not to appear on the display even after this, it requires detailed inspection.

NOTE:
- When next CE121 check is to be performed in executing secondary test, be sure to enter "A(204)=100".
- Repeat once again from the "1. Writing test data to PC1211", if the contents of PC1211 happens to change.

5-5. About repairing of CE121

Program

```
10 : PRINT #▼D▼; A(201) : PAUSE 1
 0 : GOTO 10
```

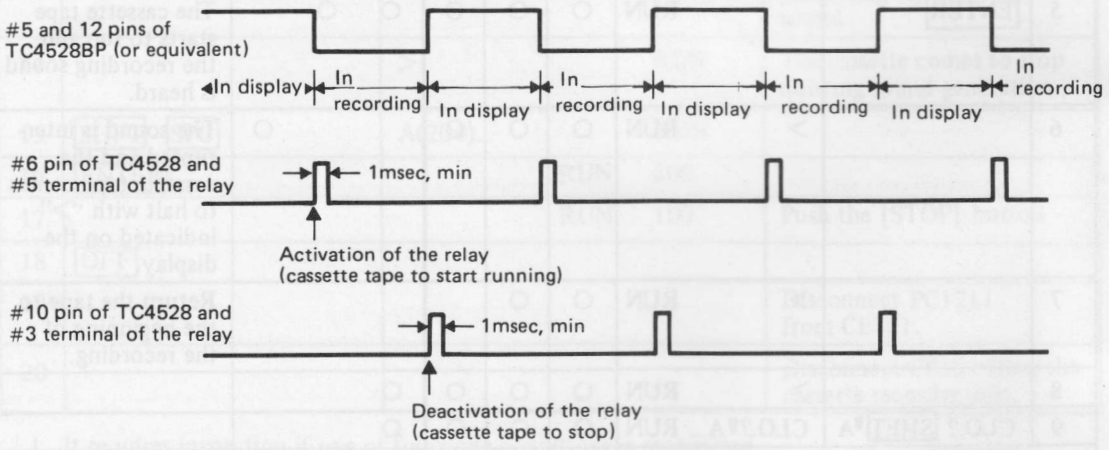
The CE121 is in proper operation if the following procedures are ended successfully.

No.	Read in	Display	Plug			Tape recorder			Remarks
			EAR PHOE	MIC	REM OTE	PLAY	REC	STOP	
1	(OFF)								Connect PC1211 with CE121.
2	ON	> RUN	○	○					Determine the location of the tape to be recorded.
3		> RUN	○	○	○	○	○		Make sure that the cassette tape does not run.
4	CS. SHIFT ▼A	CS. ▼A_ RUN	○	○	○	○	○		
5	ENTER	RUN	○	○	○	○	○		The cassette tape starts to run and the recording sound is heard.
6		> RUN	○	○	○			○	The sound is interrupted and the cassette tape comes to halt with ">" indicated on the display.
7		> RUN	○	○					Return the tape to the beginning of the recording.
8		> RUN	○	○	○	○			
9	CLO.? SHFT ▼A	CLO.?▼A_ RUN	○	○	○	○			
10	ENTER	RUN	○	○	○	○			The display contents comes to disappear from the display and the cassette tape starts to run generating the reproducing sound.
11		> RUN	○	○	○			○	Sound generation is interrupted and the cassette tape comes to halt with ">" indicated on the display.
12		RUN							
13	OFF								

[Cautions]

1. Check the machine with the check procedure provided separately, if the cassette tape happens to keep running at Step 3, the cassette tape fails to run at Step 5, or the cassette tape fails to stop at Step 6.
2. Check the recording circuit of the CE121 if no recording sound is audible at Step 5.
3. In case no reproducing sound is audible at Step 10, proceed to playback another recorded tape to check if reproducing sound is audible with that tape. If reproducing sound is not audible with that tape, proceed to check the reproducing circuit of the CE121 as it may be not functioning properly. If the reproducing sound is audible with the second tape, check the recording circuit of the CE121 as no proper recording may not have been carried out.

No.	Read in	Display		Remarks
1	RUN	RUN_	RUN	No need of running the tape recorder.
2	ENTER ←		RUN	Recording sound is audible.
3			RUN	Recording sound goes out and "10." is displayed on the display for a period of about 1 second.
4			RUN	



Cassette operation ON/OFF control must be properly executed when the above signals are observed during the execution of program.

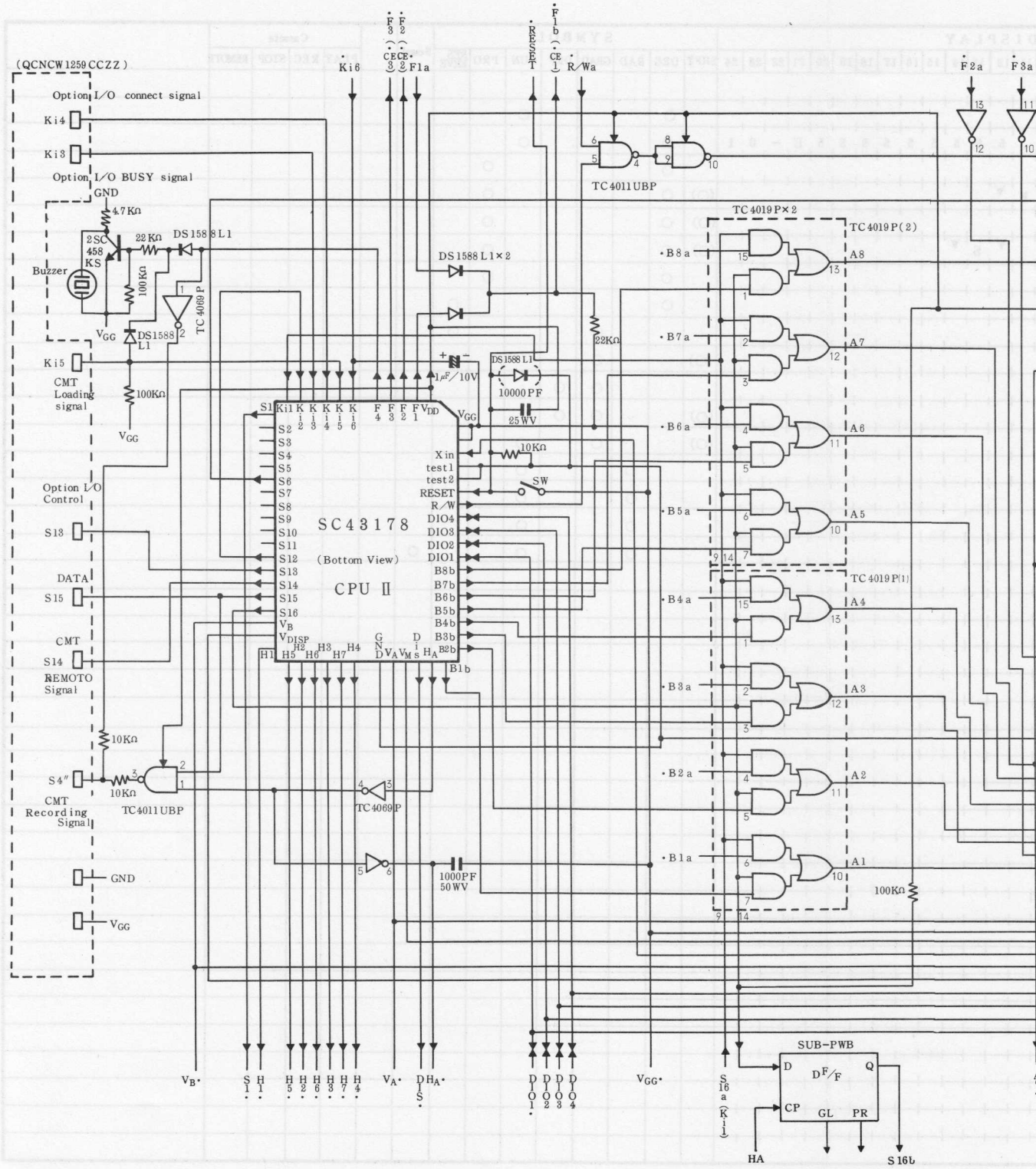
6. CHECK PROGR

		READ IN	DISPLAY
1		[ON]	>
2		[ALL RESET]	>
3		5/9 [ENTER]	5 . 5 5 5 5 5 5 5 5 5
4		[MODE]	>
5		1 P · [SHFT] W O K [SHFT] W [ENTER]	1 : P R I N T O K
6		2 [SHFT] W Z [SHFT] W P ·	2 Z P .
7		[SHFT] W S [SHFT] W [ENTER]	2 : Z P R I N T S
8		3 B E E P 2 [ENTER]	3 : B E E P 2
9		[MODE]	>
10		G R A D [ENTER]	>
11		[SHFT] [SPC] 0 1 4 7 [ENTER]	: 0 1 4 7
12		[MODE]	>
13		[SHFT] Z	S
14		[MODE] [SHFT] [SPC]	O 1 4 7
15		[CL] R A D · [ENTER]	>
16		R · [ENTER]	O K
17		[ENTER]	S
18		[ENTER]	>
19		[OFF]	
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			

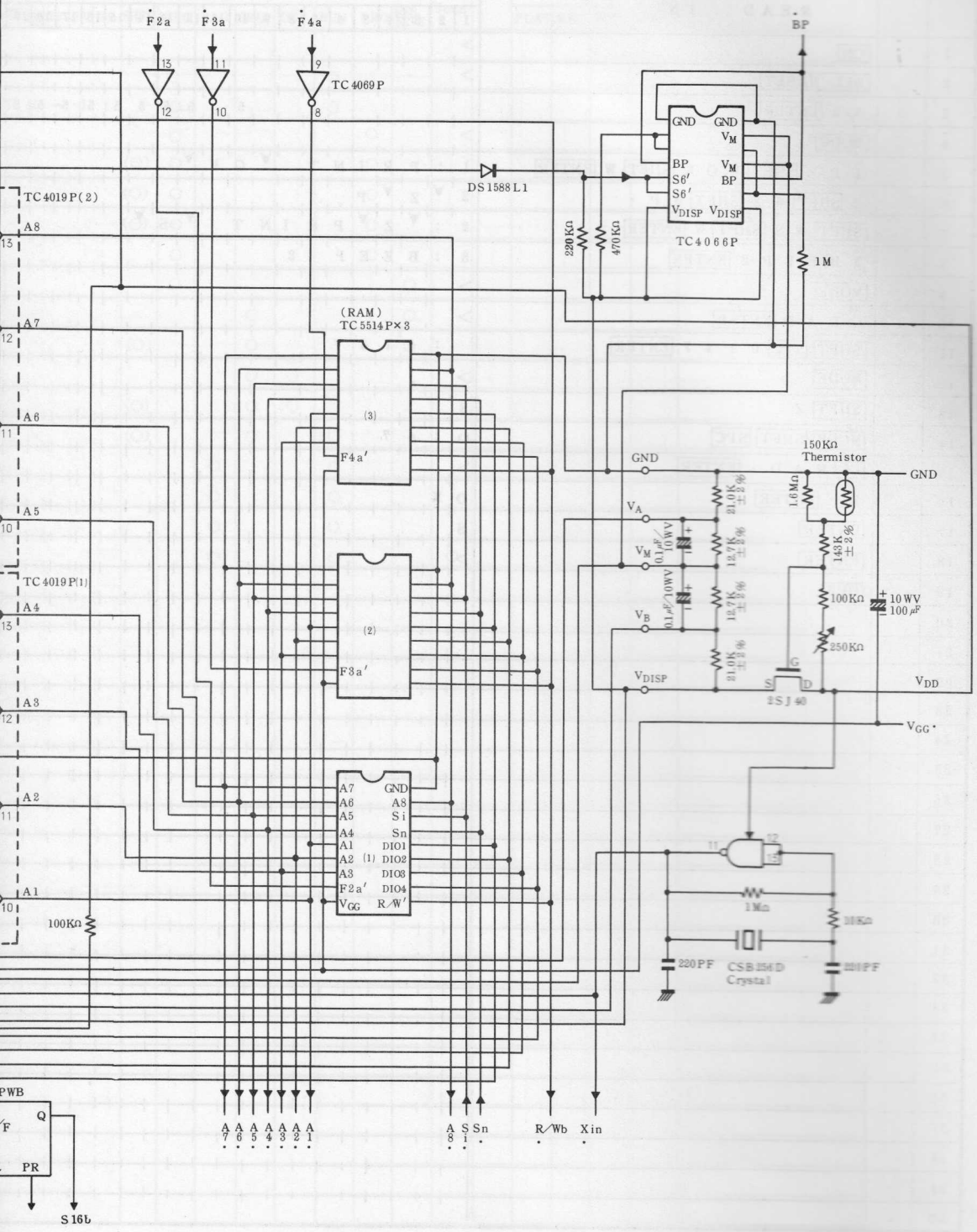
CHECK PROGRAM

DISPLAY														SYMBOL								Sound	Cassete				
11	12	13	14	15	16	17	18	19	20	21	22	23	24	SHFT	DEG	RAD	GRAD	DEF	RUN	PRO	RESERVE		PLAY	REC	STOP	REMOTE	
															○				○								
.	5	5	5	5	5	5	5	5	5	E	−	0	1		○				○								
															○					○							
K	▼													(○)	○					○							
														(○)	○					○							
	▼	S	▼											(○)	○					○							
															○					○							
															○						○						
																	○				○						
														(○)			○				○						
																	○	○									
														(○)			○	○									
														(○)			○		○								
																○			○								
																○			○								
																○			○								
																○			○			○					

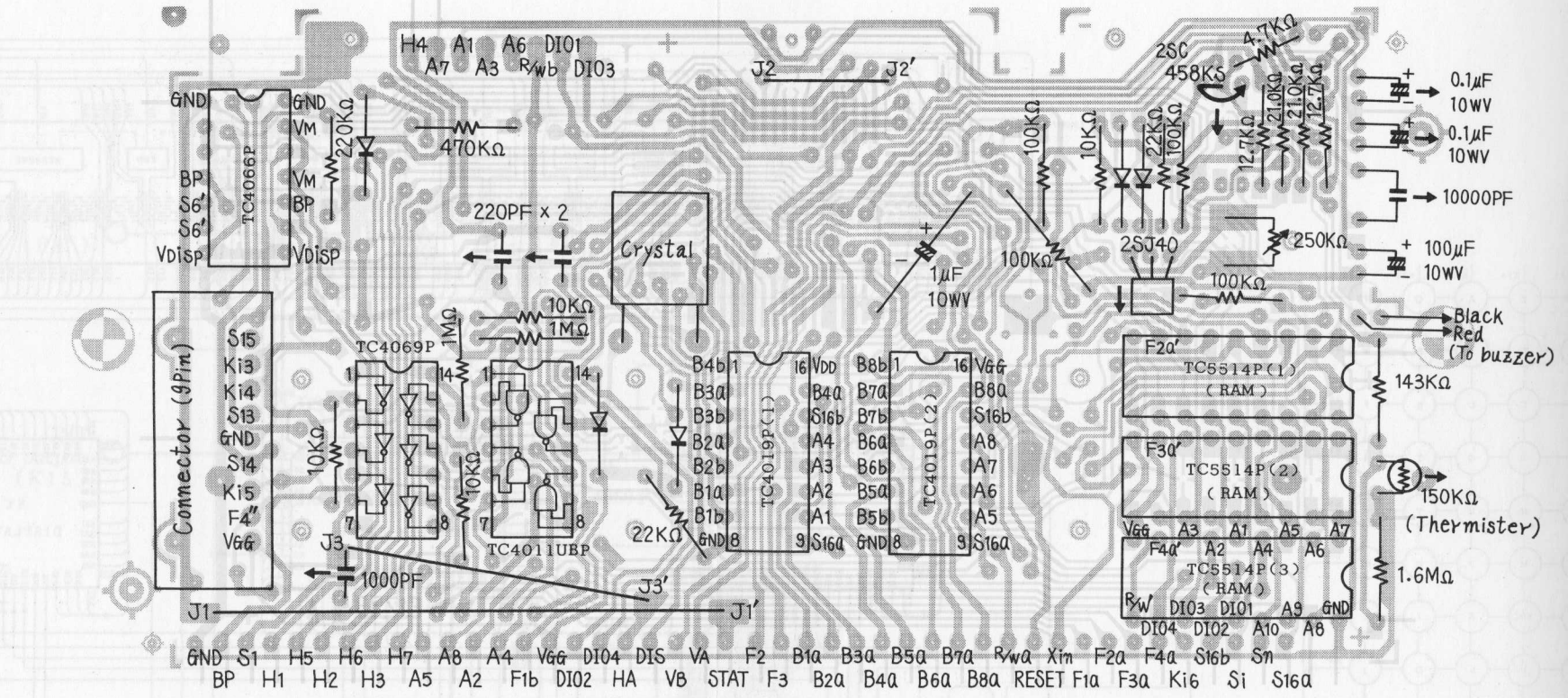
7-1. Operation Circuit Diagram



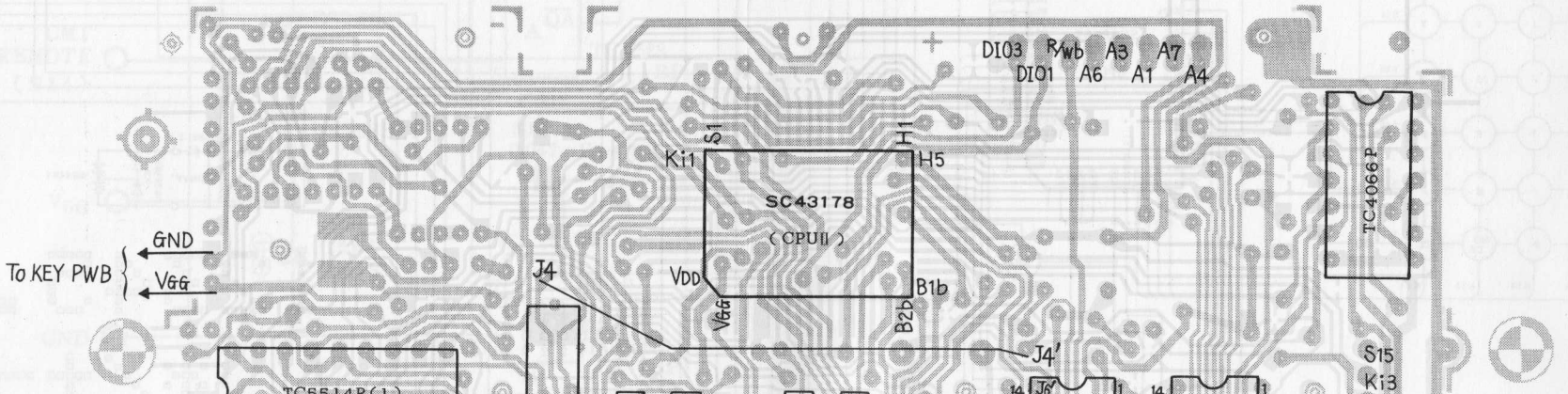
GRAM PARTS & SIGNALS POSITION

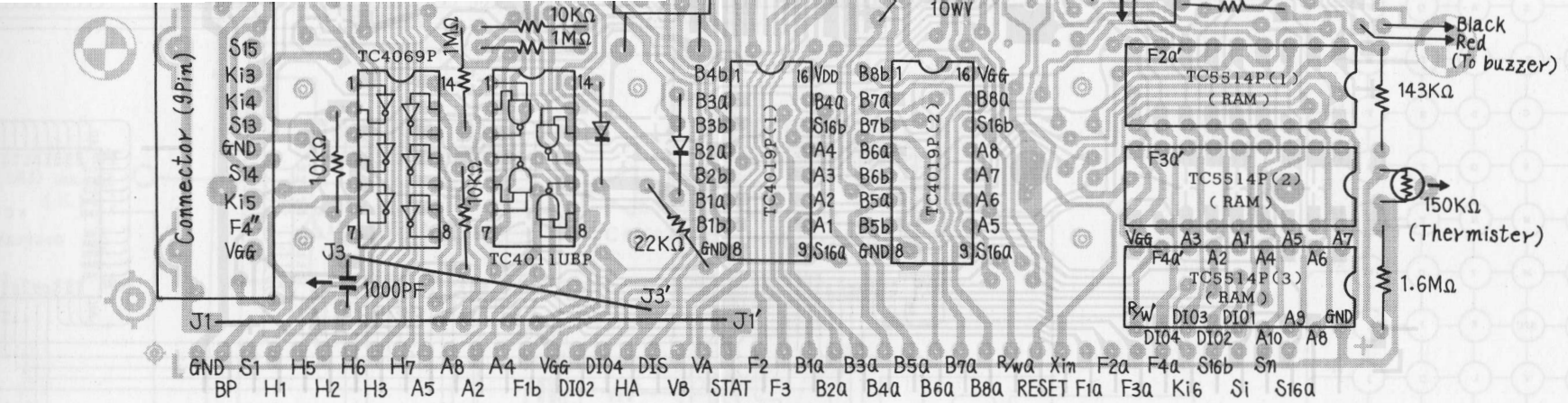


7-2. Operation P.W.B.

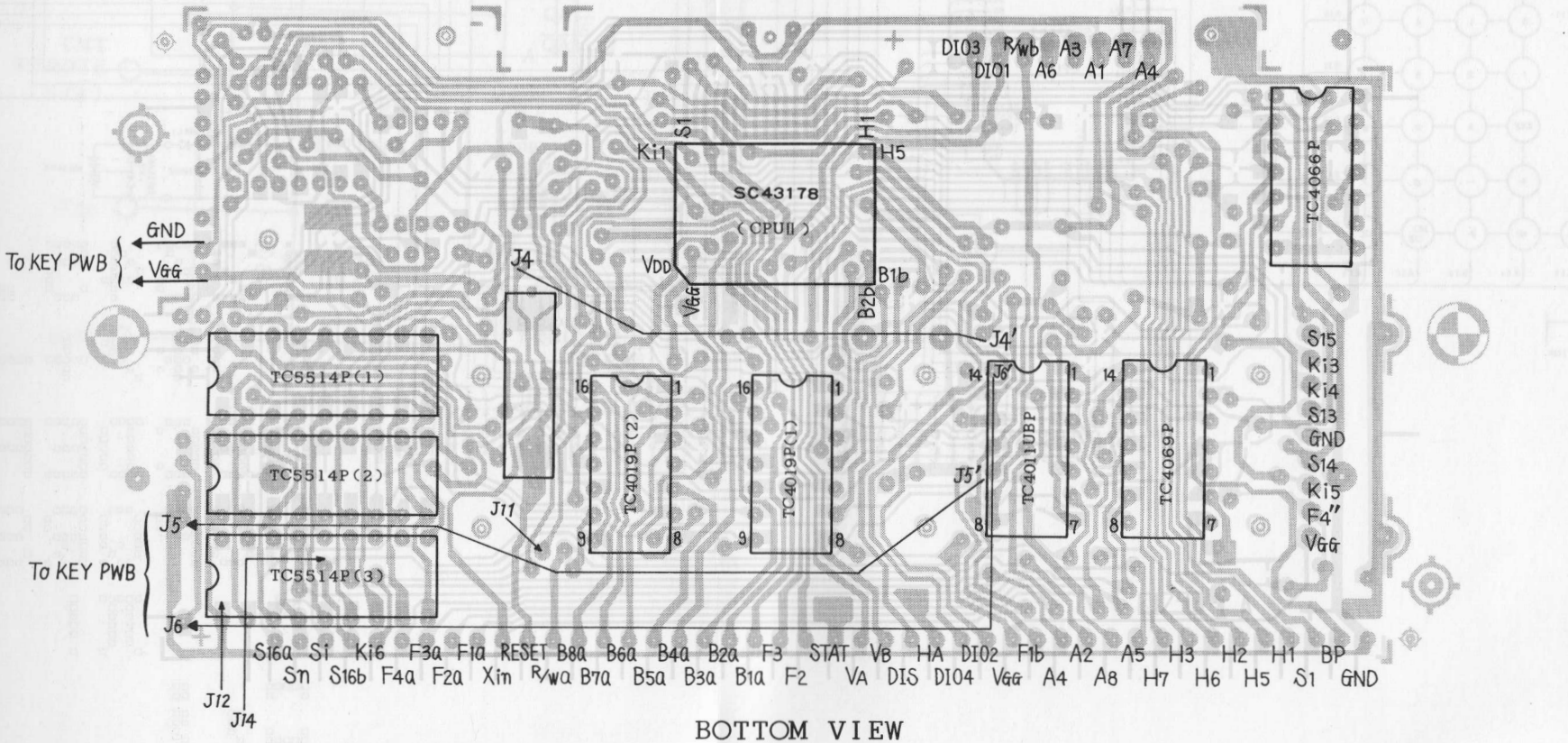


TOP VIEW



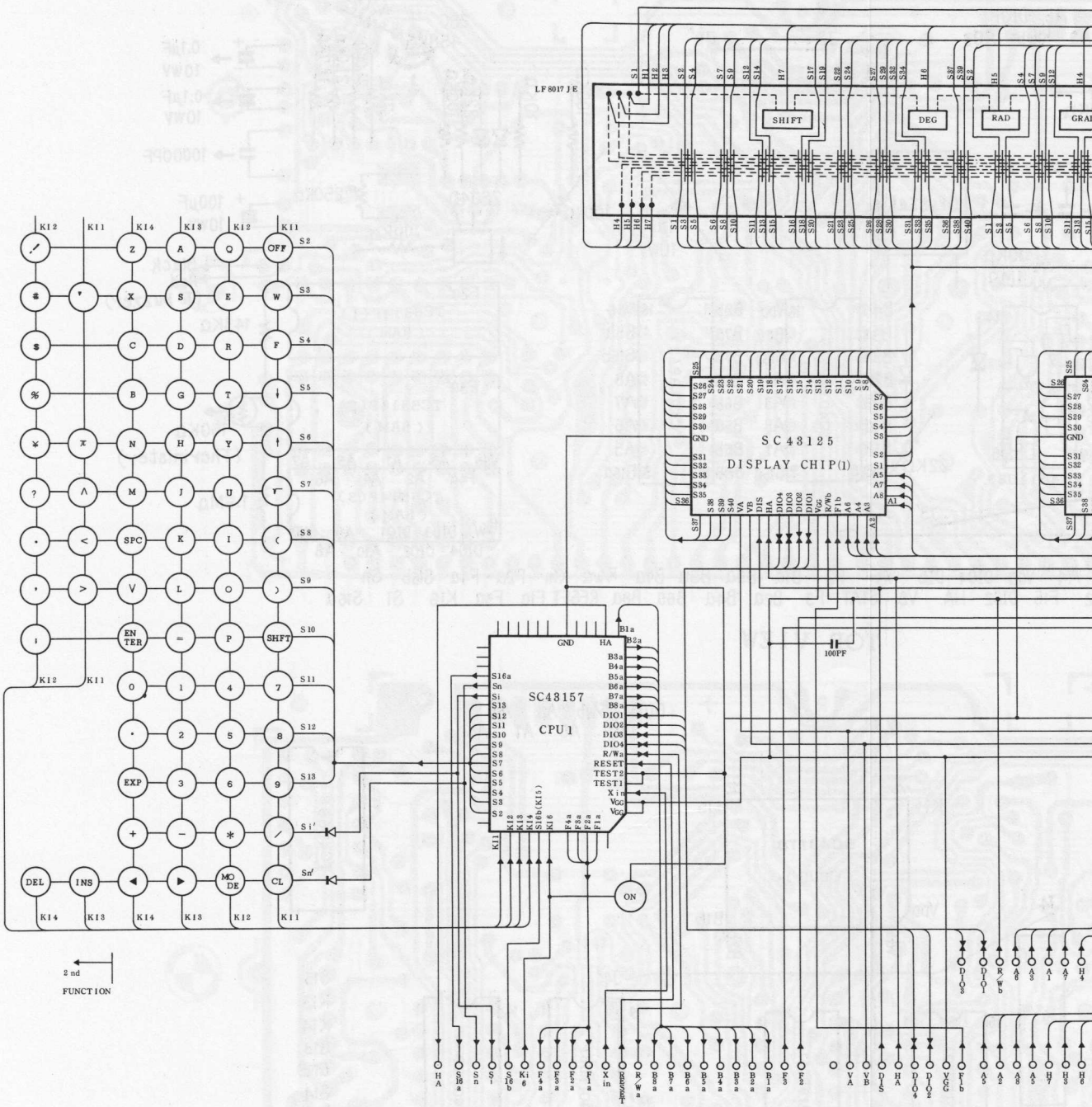


TOP VIEW

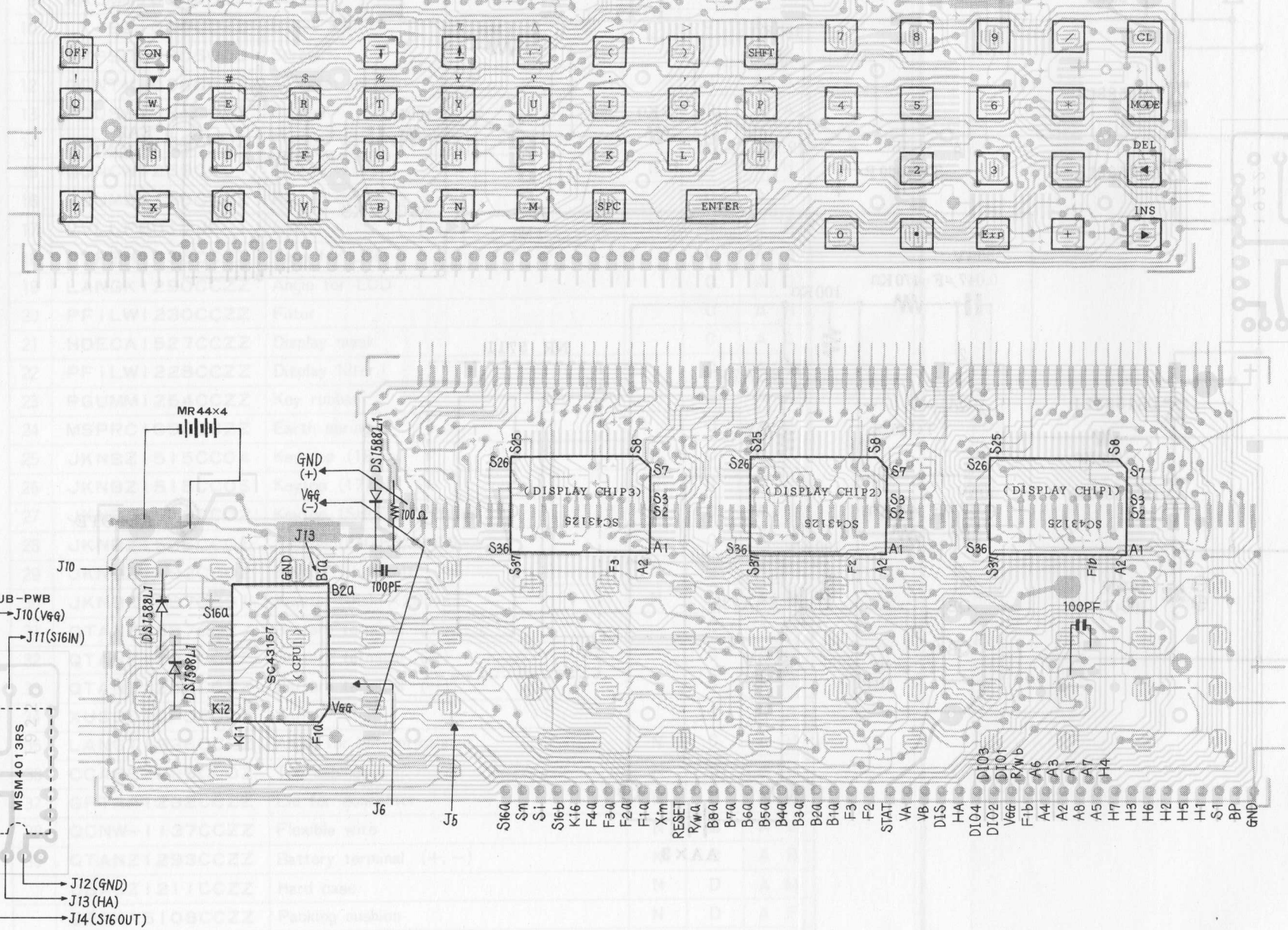


BOTTOM VIEW

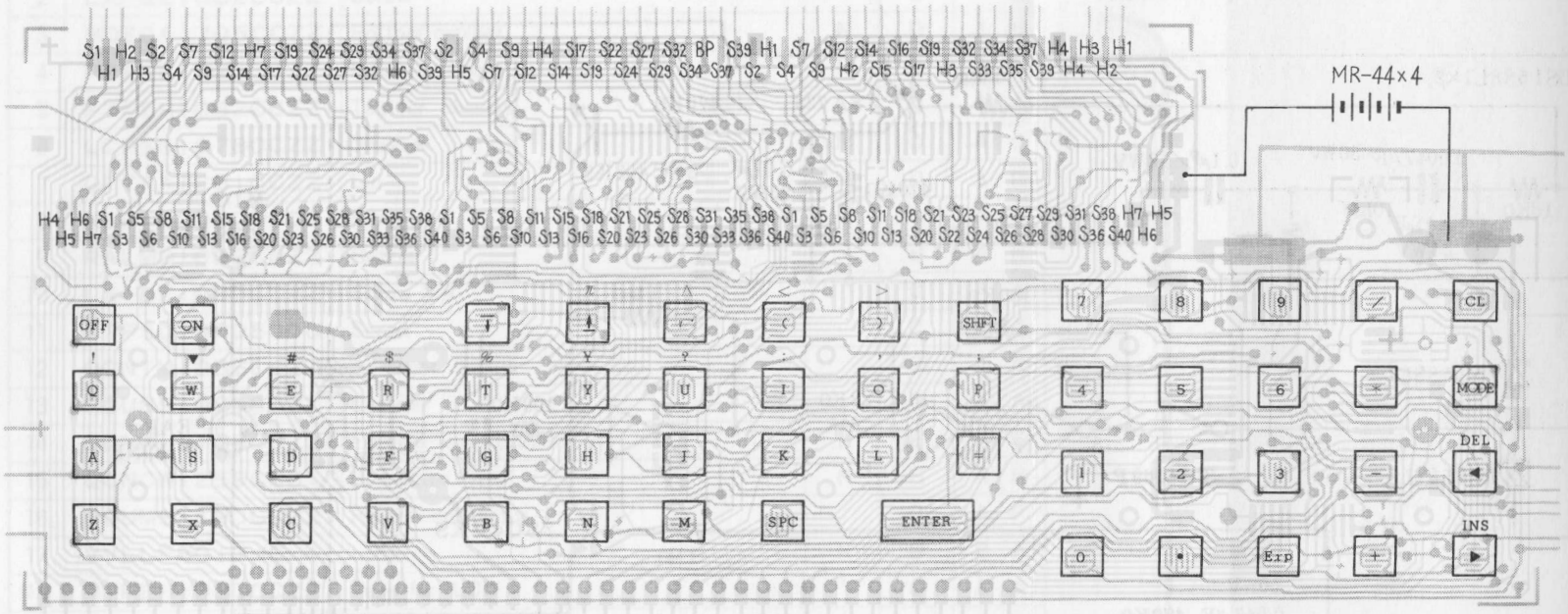
7-3. Key Circuit

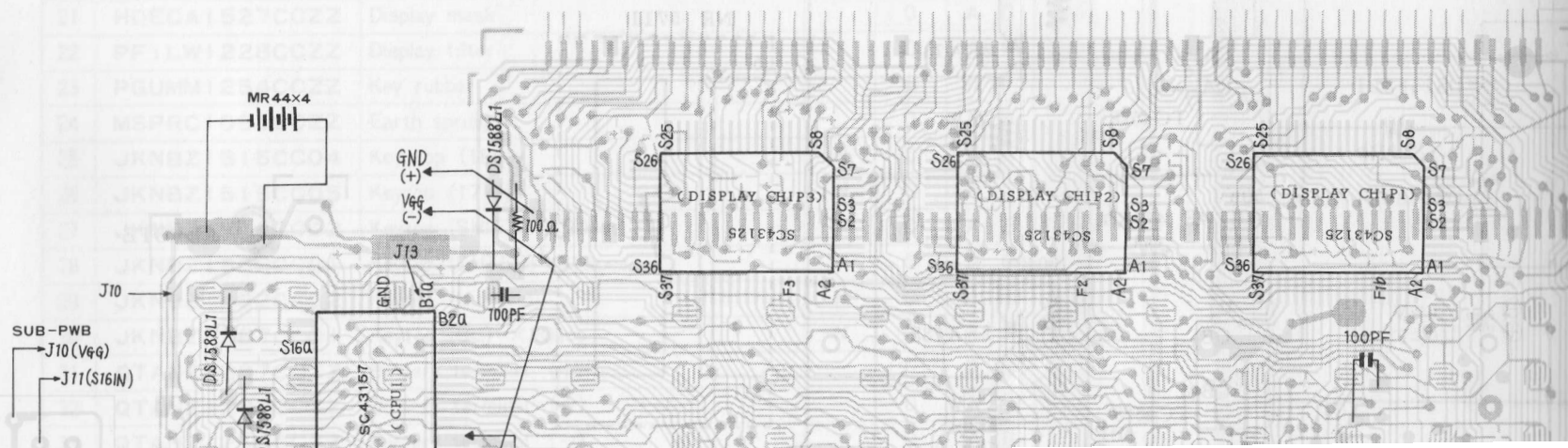


DEG
RAD
GRAD
DEF
RUN
PRO
RESERVE
SC43125
DISPLAY CHIP(2)
SC43125
DISPLAY CHIP(3)
100Ω
DS1588L1
100PF
DS1588L1
×2
MR44×4

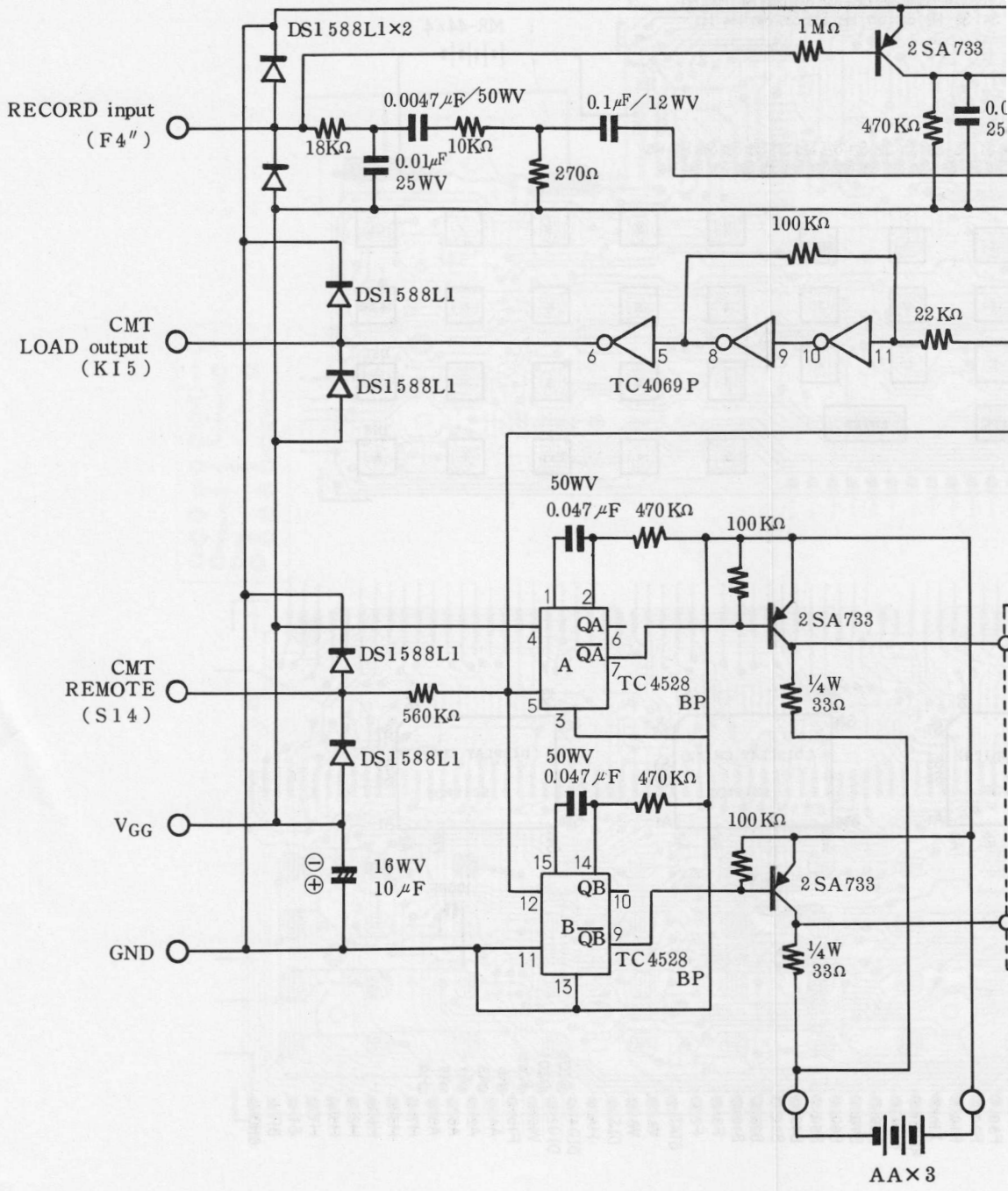

OFF
ON
SHIFT
CL
MODE
DEL
INS
ENTER
SPC
Exp
MR44×4
GND (+)
Vgg (−)
DS1588L1
100Ω
100PF
J13
J10
SUB-PWB
J10(Vgg)
J11(S16IN)
J12(GND)
J13(HA)
J14(S16OUT)
MSM4013RS
SC43167
(CPU1)
(DISPLAY CHIP3)
(DISPLAY CHIP2)
(DISPLAY CHIP1)
SC43125
J6
J5

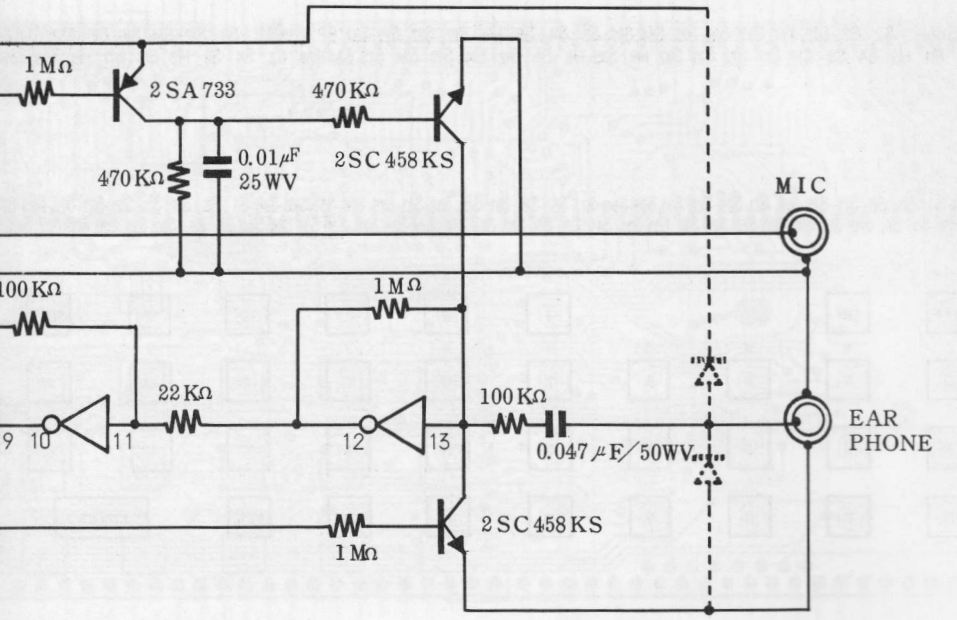
7-4. Key P.W.B.

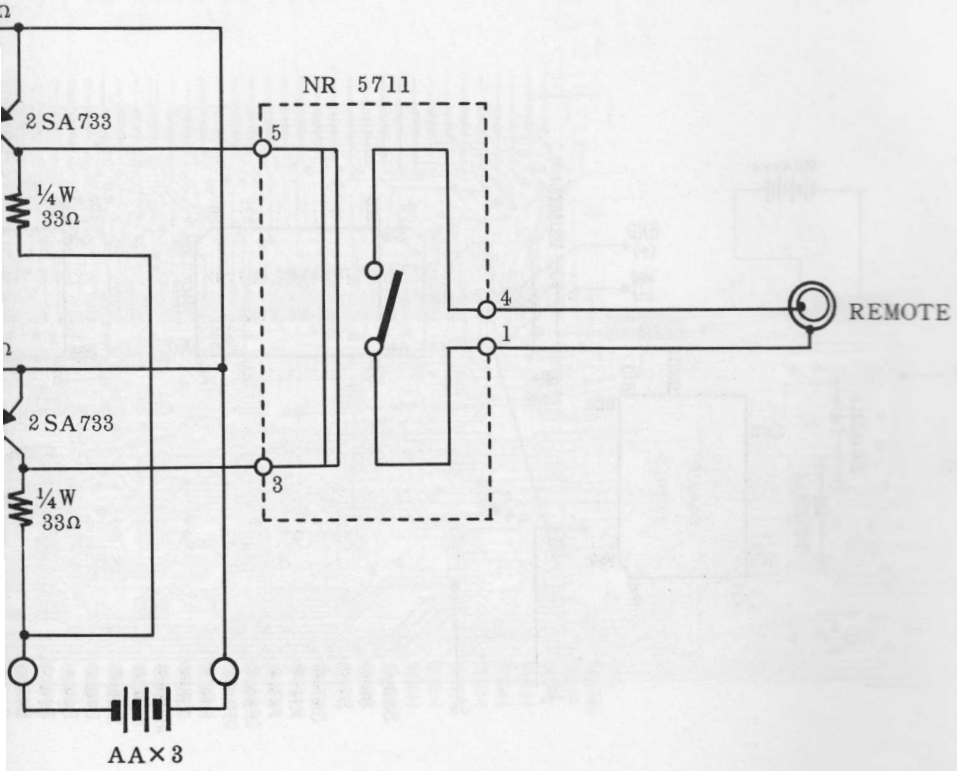

MR-44×4
OFF
ON
SHFT
CL
MODE
DEL
INS
ENTER
SPC
Q
W
E
R
T
Y
U
I
O
P
A
S
D
F
G
H
J
K
L
Z
X
C
V
B
N
M
7
8
9
4
5
6
1
2
3
0


MR44×4
GND (+)
Vgg (−)
DS1588L1
100Ω
J13
J10
SUB-PWB
J10(Vgg)
J11(S16IN)
S16Q
B1Q
B2Q
100PF
SC43157
(CPU1)
(DISPLAY CHIP3)
(DISPLAY CHIP2)
(DISPLAY CHIP1)
SC43125

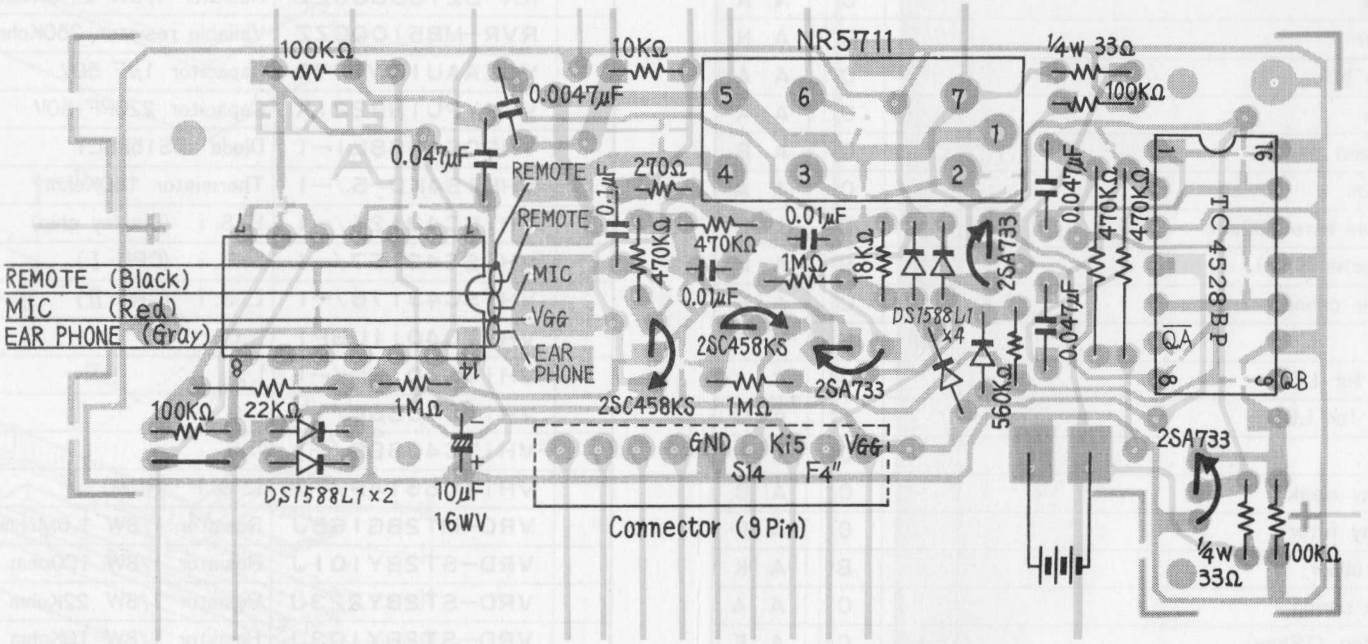
7-5. CE-121 Circuit Diagram




1MΩ
2SA733
470KΩ
470KΩ
0.01μF
25WV
2SC458KS
MIC
100KΩ
1MΩ
22KΩ
100KΩ
9
10
11
12
13
0.047μF/50WV
EAR
PHONE
2SC458KS
1MΩ


NR 5711
2SA733
5
¼W
33Ω
4
1
REMOTE
2SA733
3
¼W
33Ω
AA×3

7-6. CE-121 P.W.B.

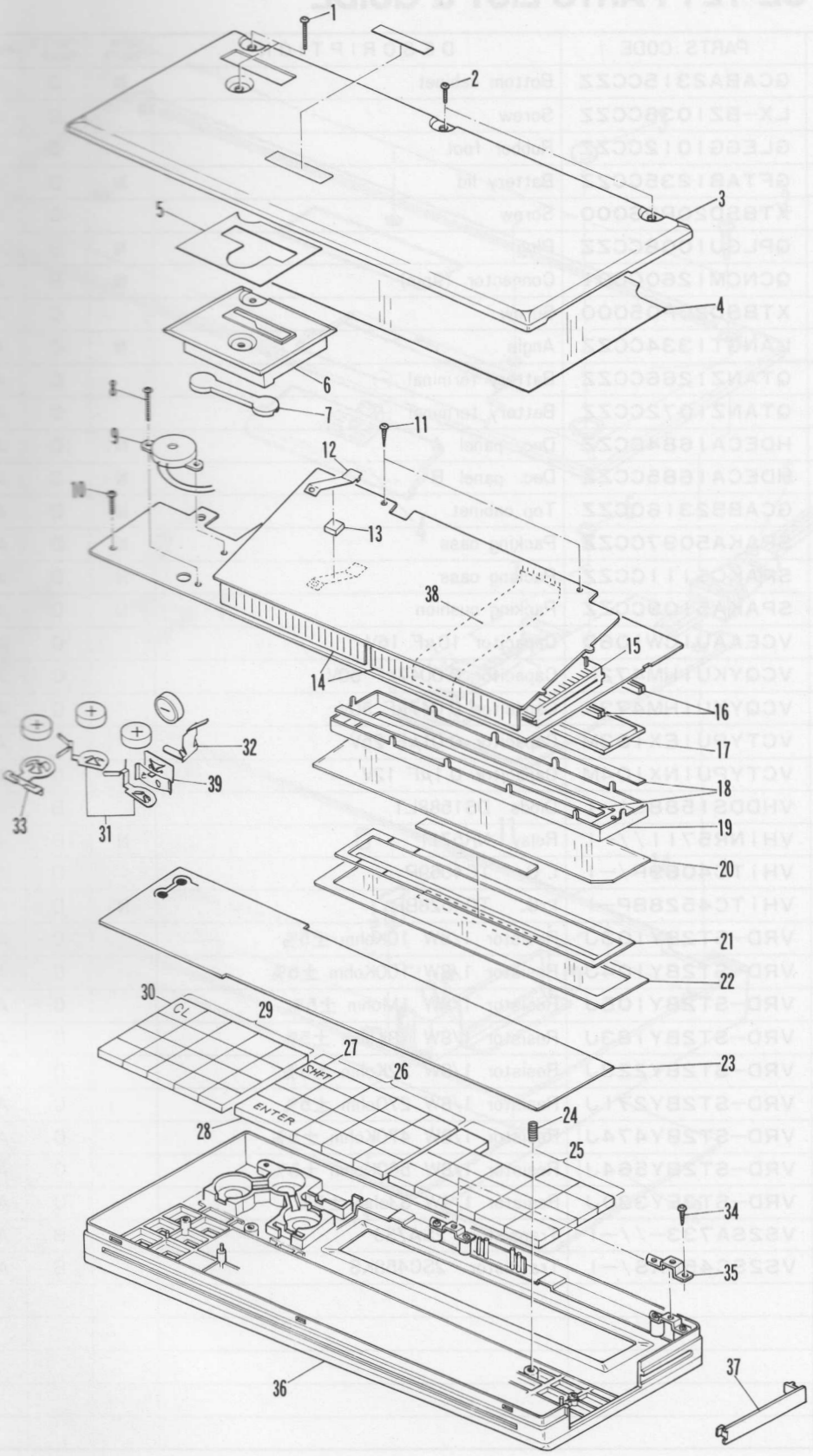

100KΩ
10KΩ
NR5711
¼w 33Ω
100KΩ
0.0047μF
0.047μF
REMOTE
REMOTE
MIC
VGG
EAR PHONE
270Ω
0.1μF
470KΩ
470KΩ
0.01μF
1MΩ
18KΩ
2SA733
DS1588L1 x4
0.01μF
2SC458KS
2SA733
2SC458KS
1MΩ
560KΩ
0.047μF
470KΩ
470KΩ
TC4528BP
QA
QB
REMOTE (Black)
MIC (Red)
EAR PHONE (Gray)
100KΩ
22KΩ
1MΩ
DS1588L1x2
10μF
16WV
GND
Ki5
VGG
S14
F4"
Connector (9 Pin)
2SA733
¼w 33Ω
100KΩ

8. PC-1211 PARTS LIST & GUIDE

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
1	LX-BZ1102CCZZ	Screw	N	C	A B
2	LX-BZ1032CCZZ	Screw		C	A A
3	HDECA1705CCZZ	Bottom cabinet	N	D	A N
4	PZETL1323CCZZ	Insulator sheet	N	C	A B
5	PTPEH1062CCZZ	Tap for chassis		C	A A
6	LCHSS1078CCZZ	Chassis	N	C	A C
7	GFTAA1231CCZZ	Lid	N	D	A B
8	XBPSD20P09000	Screw		C	A A
9	RALMB1006CCZZ	Buzzer		B	A H
10	LX-BZ1060CCZZ	Screw ×9		C	A A
11	XTPSD20P05000	Screw		C	A A
12	QCNTM1036CCZZ	All reset switch		C	A B
13	PCUSS1081CCZZ	Cushion		C	A A
14	QCNW-1135CCZZ	Flexible wire (22pin)	N	B	A C
15	QCNCW1259CC0i	Connector (9pin)	N	B	A H
16	PGUMS1190CCZZ	Rubber connector		C	A F
17	VVLLF8017JE-1	LCD	N	B	B A
18	PTPEH1033CCZZ	Tape for LCD		C	A A
19	LANGK1290CCZZ	Angle for LCD		C	A D
20	PFiLW1230CCZZ	Filter		C	A H
21	HDECA1527CCZZ	Display mask		C	A C
22	PFiLW1228CCZZ	Display filter		C	A C
23	PGUMM1254CCZZ	Key rubber		B	A K
24	MSPRC1098CCZZ	Earth spring		C	A A
25	JKNBZ1515CC04	Key top (18key)	N	C	A F
26	JKNBZ1515CC05	Keytop (17key)	N	C	A F
27	JKNBZ1516CC02	Keytop (SHIFT) ×20pcs	N	C	A E
28	JKNBZ1566CC01	Keytop (ENTER) ×10pcs	N	C	A G
29	JKNBZ1492CC02	Keytop (Numeral)	N	C	A E
30	JKNBZ1567CC01	Keytop (CL) ×20pcs	N	C	A E
31	QTANZ1287CCZZ	Battery terminal (+, −)		C	A B
32	QTANZ1292CCZZ	Battery terminal (+)		C	A B
33	QTANZ1250CCZZ	Battery terminal (−)		C	A B
34	XUSSD20P04000	Screw		C	A A
35	LANGT1336CCZZ	Angle for bottom cabinet	N	C	A B
36	CCABB2299CC02	Top cabinet	N	D	A S
37	GFTAA1232CCZZ	Lid for connector	N	D	A B
38	QCNW-1137CCZZ	Flexible wire	N	B	A C
39	QTANZ1293CCZZ	Battery terminal (+, −)	N	C	A B
	UBAGZ1211CCZZ	Hard case	N	D	A M
	SPAKA5108CCZZ	Packing cushion	N	D	A F
	TiNSE3137CCZZ	Instruction book (U.S.A)	N	D	A P

NO.	PART
	TMANE1
	SPAKC5
	TiNSE2
	LPLTP1
	TLABZ1
	RR-DZ1
	RR-DZ1
	RR-DZ1
	RVR-ME
	VCEAAU
	VCKYPU
	VHDDS1
	VHH154
	VHiSC4
	VHiSC4
	VHiSC4
	VHiTC4
	VHiTC4
	VHiTC4
	VHiTC4
	VHiTC5
	VRC-MT
	VRD-ST
	VRD-ST
	VRD-ST
	VRD-ST
	VRD-ST
	VRD-ST
	VRD-ST
	VS2SC4
	VS2SJ4
	RC-SZ1
	RCRSP1
	VCKYPU
	VCTYPU
	RC-SZ1
	VRD-ST
	VCKYPU
	DKiT-1

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
	TMANE1010CCZZ	Program library	N	D	A Z
	SPAKC5012CCZZ	Packing case	N	D	A G
	TiNSE2826CCZZ	Basic text	N	D	A K
	LPLTP1070CCZZ	Tenplate	N	D	A B
	TLABZ1295CCZZ	Name lavel		D	A A
	RR-DZ1006CCZZ	Resistor 1/8W 143Kohm ±2%		C	A B
	RR-DZ1007CCZZ	Resistor 1/8W 12.7Kohm ±2%		C	A B
	RR-DZ1008CCZZ	Resistor 1/8W 21.0Kohm ±2%		C	A B
	RVR-MB510QCZZ	Valiable resistor 250Kohm		C	A D
	VCEAAU1AW107Q	Capacitor 1μF 50V		C	A E
	VCKYPU1HB221K	Capacitor 220PF 50V		C	A B
	VHDDS1588L1-1	Diode DS1588L1		B	A D
	VHH154KD-5/-1	Thermistor 150Kohm		B	A C
	VHiSC4325/-1	L. S. i (Display chip)		B	A X
	VHiSC4357/-1	L. S. i (CPU-Ⅰ)	N	B	B F
	VHiSC4378/-1	L. S. i (CPU-Ⅱ)	N	B	B D
	VHiTC4011UBP1	i. C.		B	A F
	VHiTC4019P/-1	i. C.		B	A K
	VHiTC4066P/-1	i. C.		B	A K
	VHiTC4069P/-1	i. C.		B	A H
	VHiTC5514P/-1	L. S. i (RAM)		B	B D
	VRC-MT2BG165J	Resistor 1/8W 1.6Mohm ±5%		C	A B
	VRD-ST2BY101J	Resistor 1/8W 100ohm ±5%		C	A A
	VRD-ST2BY223J	Resistor 1/8W 22Kohm ±5%		C	A A
	VRD-ST2BY103J	Resistor 1/8W 10Kohm ±5%		C	A A
	VRD-ST2BY104J	Resistor 1/8W 100Kohm ±5%		C	A A
	VRD-ST2BY105J	Resistor 1/8W 1Mohm ±5%		C	A A
	VRD-ST2BY472J	Resistor 1/8W 4.7Kohm ±5%		C	A A
	VRD-ST2BY474J	Resistor 1/8W 470Kohm ±5%		B	A A
	VS2SC458KS/-1	Transistor 2SC458KS		B	A C
	VS2SJ40-///-1	MOS FET 2SJ40		C	A G
	RC-SZ1005CCZZ	Capacitor 0.1μF 10V		C	A C
	RCRSP1024CCZZ	Crystal	N	C	A H
	VCKYPU1HB101K	Capacitor 100PF 50V		C	A A
	VCTYPU1EX103M	Capacitor 10000PF 25V		C	A B
	RC-SZ1007CCZZ	Capacitor 1μF 10V		C	A F
	VRD-ST2BY224J	Resistor 1/8W 220Kohm ±5%		C	A A
	VCKYPU1HB102K	Capacitor 1000PF 50V		C	A A
	DKiT-1001CCZZ	SUB-PWB Kit	N		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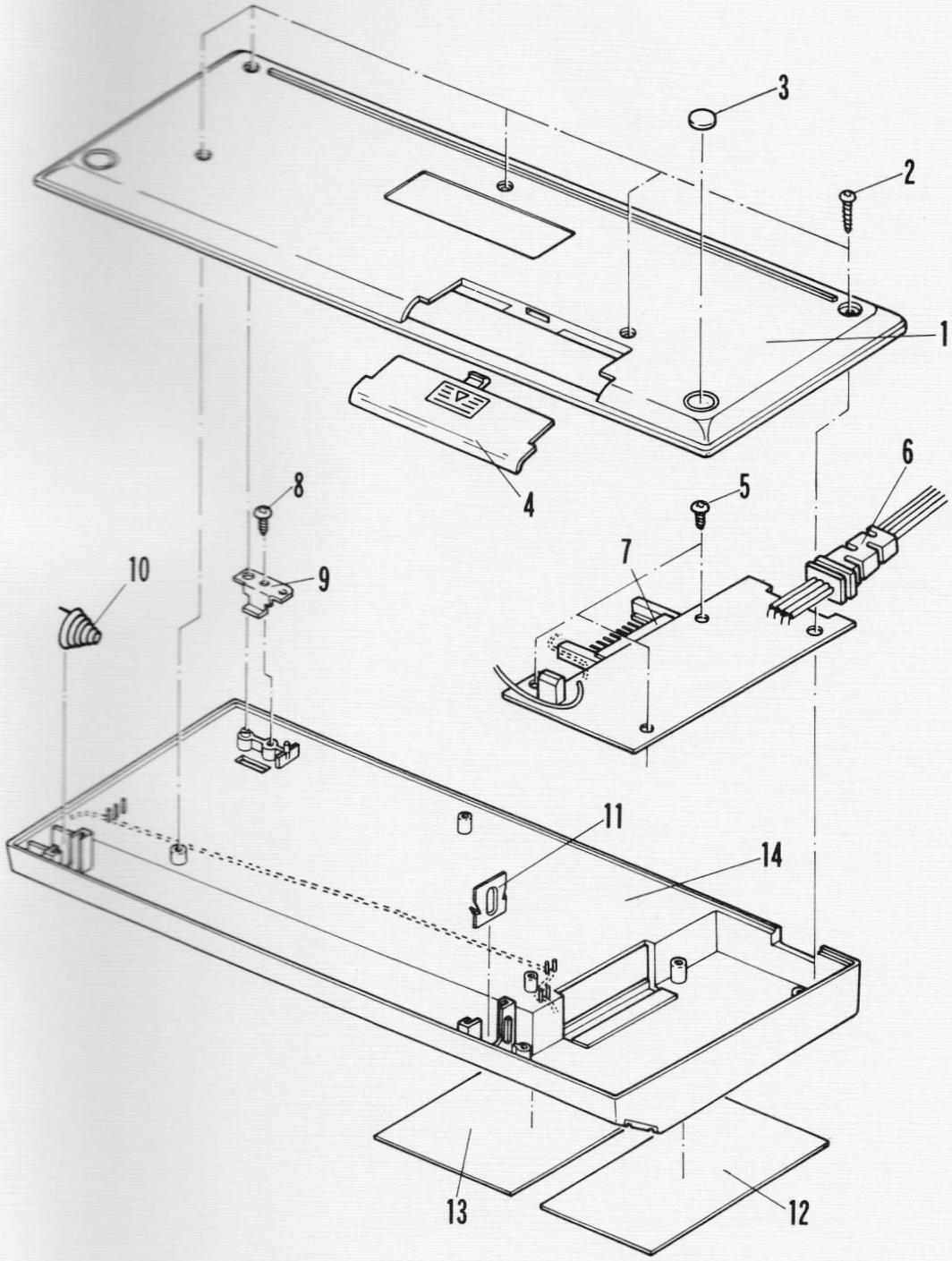
9. CE-121 PARTS LIST & GUIDE

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
1	GCABA2315CCZZ	Bottom cabinet	N	D	A G
2	LX-BZ1038CCZZ	Screw		C	A A
3	GLEGG1012CCZZ	Rubber foot		C	A A
4	GFTAB1235CCZZ	Battery lid	N	D	A C
5	XTBSD20P06000	Screw		C	A A
6	QPLGJ1008CCZZ	Plug	N	B	A Q
7	QCNCM1260CC01	Connector (9pin)	N	B	A G
8	XTBSD20P05000	Screw		C	A A
9	LANGT1334CCZZ	Angle	N	C	A C
10	QTANZ1266CCZZ	Battery terminal ⊖		C	A A
11	QTANZ1072CCZZ	Battery terminal ⊕		C	A A
12	HDECA1684CCZZ	Dec. panel A	N	D	A C
13	HDECA1685CCZZ	Dec. panel B	N	D	A D
14	GCABB2316CCZZ	Top cabinet	N	D	A G
	SPAKA5097CCZZ	Packing case	N	D	A D
	SPAKC5111CCZZ	Packing case	N	D	A D
	SPAKA5109CCZZ	Packing cushion	N	D	A E
	VCEAAU1CW106Q	Capacitor 10μF 16V		C	A B
	VCQYKU1HM472K	Capacitor 0.0047μF 50V		C	A B
	VCQYKU1HM473K	Capacitor 0.047μF 50V		C	A B
	VCTYPU1EX103M	Capacitor 0.01μF 25V		C	A B
	VCTYPU1NX104M	Capacitor 0.1μF 12V		C	A B
	VHDDS1588L1-1	Diode DS1588L1		B	A B
	VHiNR5711//-1	Relay NR5711	N	B	A W
	VHiTC4069P/-1	I. C. TC4069P		B	A H
	VHiTC4528BP-1	I. C. TC4528BP	N	B	A P
	VRD-ST2BY103J	Resistor 1/8W 10Kohm ±5%		C	A A
	VRD-ST2BY104J	Resistor 1/8W 100Kohm ±5%		C	A A
	VRD-ST2BY105J	Resistor 1/8W 1Mohm ±5%		C	A A
	VRD-ST2BY183J	Resistor 1/8W 18Kohm ±5%		C	A A
	VRD-ST2BY223J	Resistor 1/8W 22Kohm ±5%		C	A A
	VRD-ST2BY271J	Resistor 1/8W 270ohm ±5%		C	A A
	VRD-ST2BY474J	Resistor 1/8W 470Kohm ±5%		C	A A
	VRD-ST2BY564J	Resistor 1/8W 560Kohm ±5%		C	A A
	VRD-ST2EY330J	Resistor 1/4W 33ohm ±5%		C	A A
	VS2SA733-//-1	Transistor 2SA733		B	A D
	VS2SC458KS/-1	Transistor 2SC458KS		B	A C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