# SHARP SERVICE MANUAL

CODE: 00ZPC1251///E


# PC-1251

## MODEL PC-1250

CONTENTS



☆ Difference between PC1250 and PC1251:

Program data area of the PC-1251 is larger by 2048 bytes.

☆ CE-125 option:

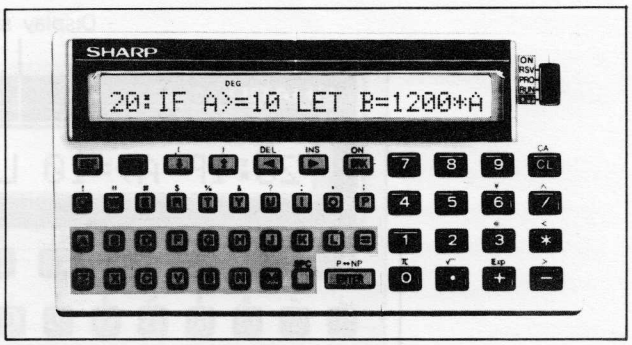
Microcassette tape recorder is available as an external memory device and 24-digit thermal dot printer is incorporated as the output device.

SHARP CORPORATION

# 1. iNTRODUCTiON TO THE PC-1251

The **SHARP PC-1251** system consists of:

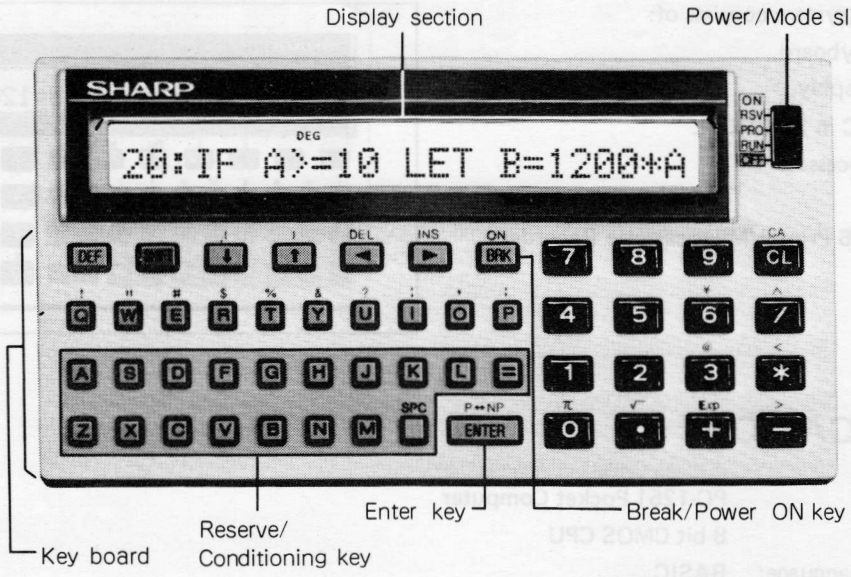
- ★ 52-character keyboard.
- ★ 24-character display.
- ★ Powerful BASIC in 24K ROM.
- ★ 8 bit CMOS processor.
- ★ 4KB RAM.
- ★ Optional **CE-125** Printer/Microcassette Recorder.



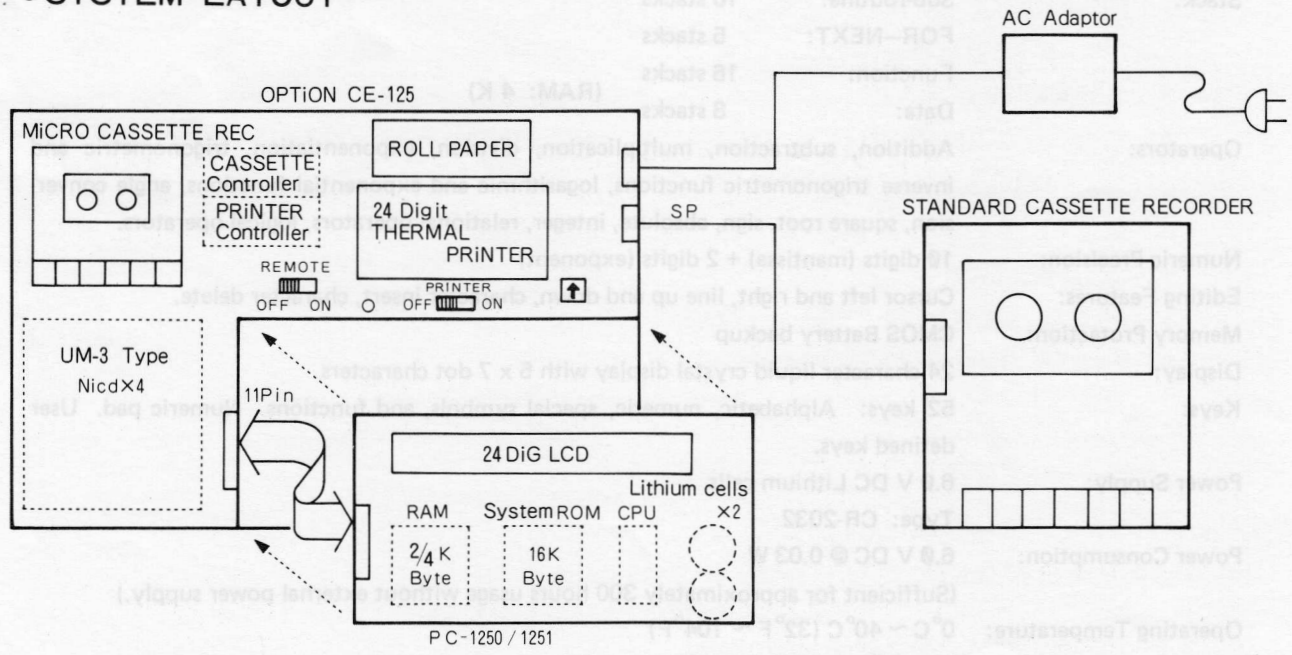

# 2. SPECiFiCATiON

| | | |
|---|---|---|
| Model: | PC-1251 Pocket Computer | |
| Processor: | 8 bit CMOS CPU | |
| Programming Language: | BASIC | |
| Memory Capacity: | System ROM: | 24 K Bytes |
| | RAM | |
| | System | About 500 Bytes |
| | User | |
| | Fixed Memory Area (A ~ Z, A$ ~ Z$) | 208 Bytes |
| | Reserve Area | 48 Bytes |
| | Program/Data Area | 3486 Bytes |
| Stack: | Sub-routine: 10 stacks | |
| | FOR–NEXT: 5 stacks | |
| | Function: 16 stacks | (RAM: 4 K) |
| | Data: 8 stacks | |
| Operators: | Addition, subtraction, multiplication, division, exponentiation, trigonometric and inverse trigonometric functions, logarithmic and exponential functions, angle conversion, square root, sign, absolute, integer, relational operators, logical operators. | |
| Numeric Precision: | 10 digits (mantissa) + 2 digits (exponent) | |
| Editing Features: | Cursor left and right, line up and down, character insert, character delete. | |
| Memory Protection: | CMOS Battery backup | |
| Display: | 24 character liquid crystal display with 5 x 7 dot characters | |
| Keys: | 52 keys: Alphabetic, numeric, special symbols, and functions. Numeric pad. User defined keys. | |
| Power Supply: | 6.0 V DC Lithium cells<br>Type: CR-2032 | |
| Power Consumption: | 6.0 V DC @ 0.03 W<br>(Sufficient for approximately 300 hours usage without external power supply.) | |
| Operating Temperature: | 0°C ~ 40°C (32°F ~ 104°F) | |
| Dimensions: | 135 (W) x 70 (D) x 9.5 (H) mm<br>5-5/16″ (W) x 2-3/4″ (D) x 3/8″ (H) | |
| Weight: | Approximately 115 g (0.25 lbs) (with cells) | |
| Accessories: | Wallet, two lithium cells (built-in), two keyboard templates and instruction manual | |
| Options: | Printer/Microcassette Recorder (CE-125) | |

## • KEY LAYOUT




## • SYSTEM LAYOUT

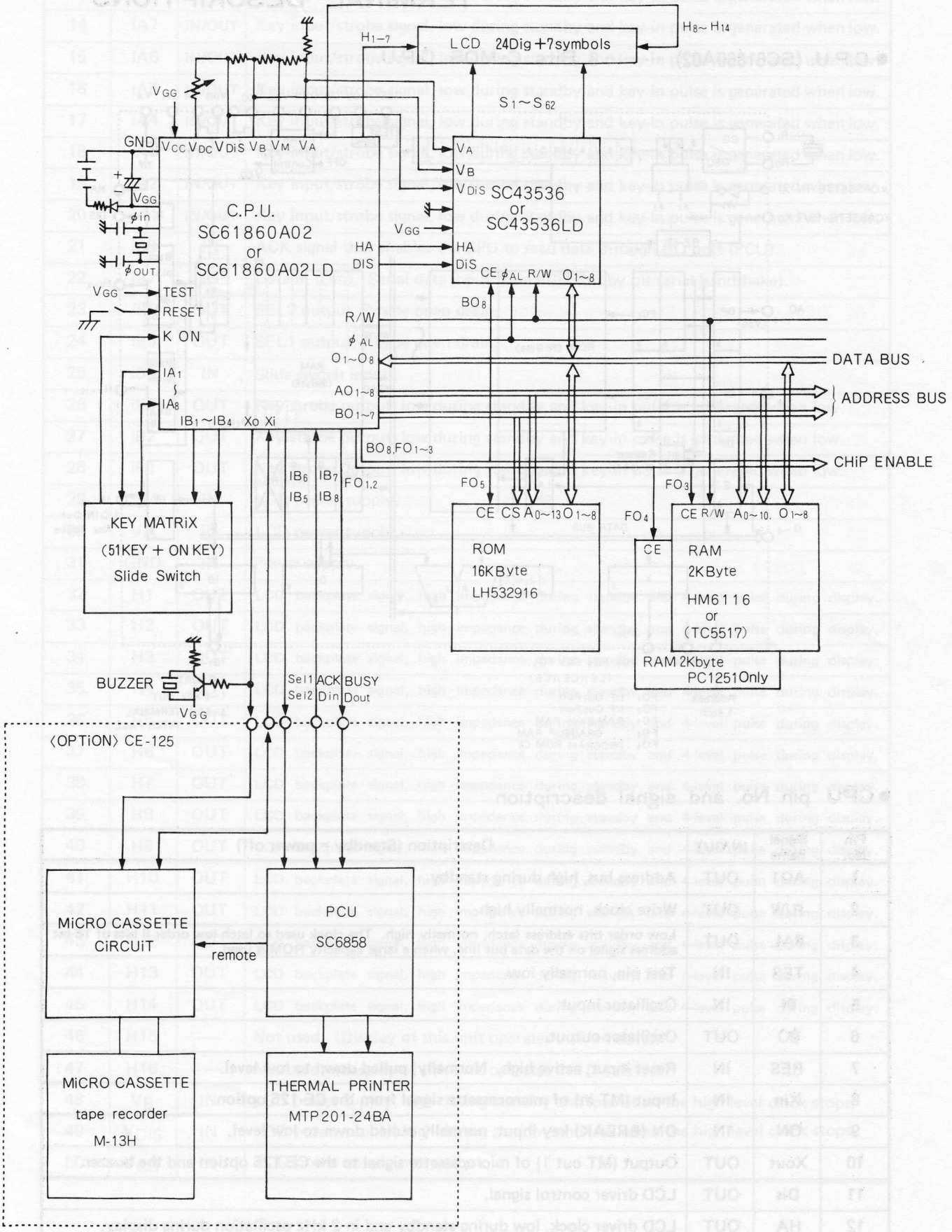



NOTE:

Standard cassette tape recorder can only be used to write data to the computer via the CE-125.

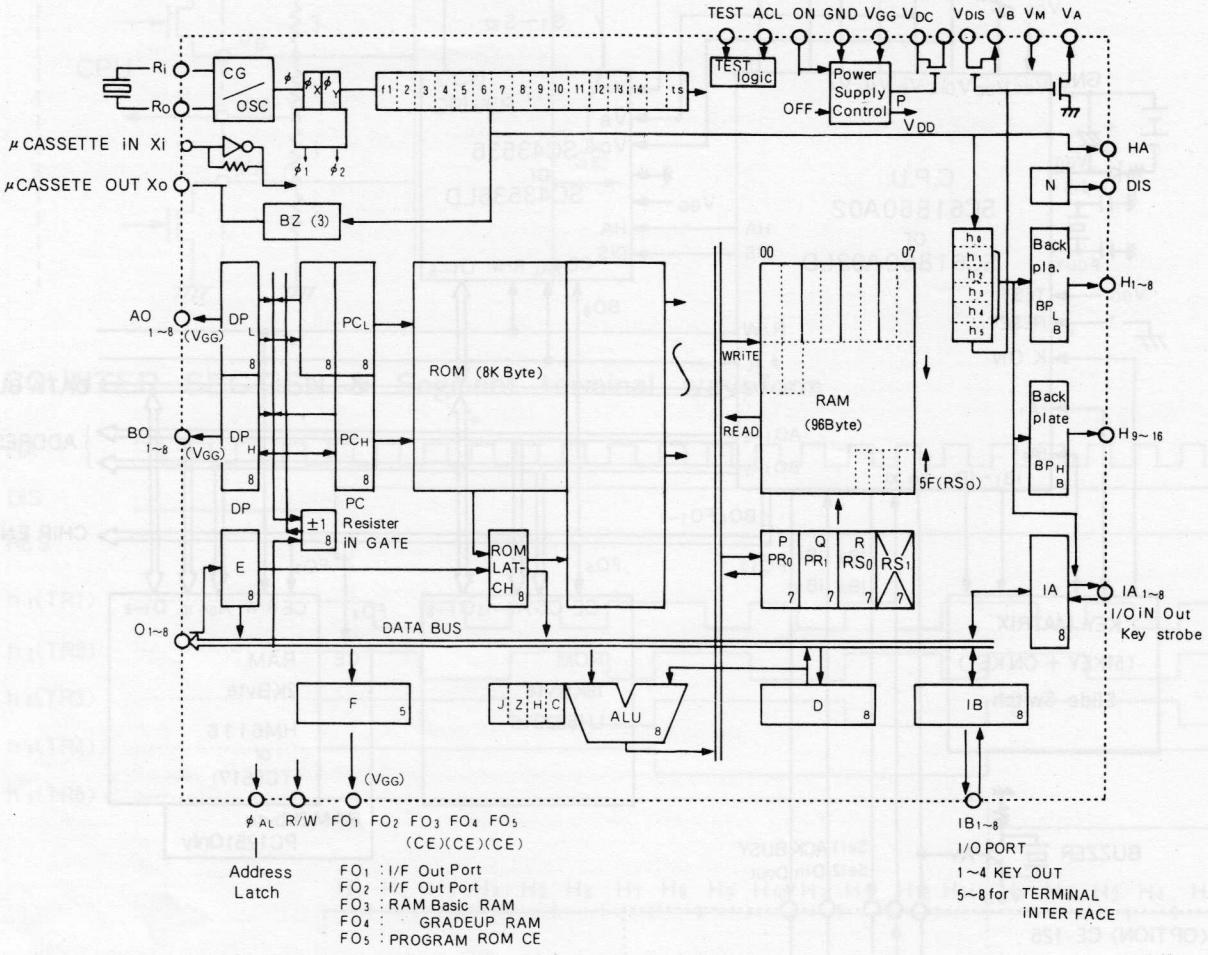
Recording to the standard cassette tape is not possible.

# 3. PC-1250 / PC-1251 SYSTEM BLOCK DiAGRAM



# 4. C.P.U.iNTERNAL BLOCK DiAGRAM & TERMiNAL DESCRiPTiONS

● C.P.U. (SC61860A02) ····· 8 Bits C-MOS C.P.U.




● CPU pin No. and signal description

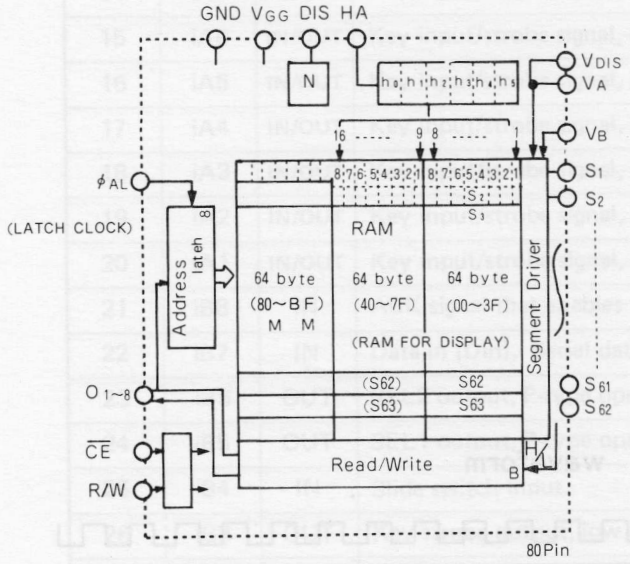
| Pin No. | Signal name | IN/OUT | Description (Standby = power off) |
|---|---|---|---|
| 1 | AO1 | OUT | Address bus, high during standby. |
| 2 | R/W | OUT | Write clock, normally high. |
| 3 | ØAL | OUT | Low order bits address latch, normally high. The clock used to latch low order 8 bits of 16-bit address signal on the data bus line, when a large capacity ROM is used. |
| 4 | TES | IN | Test pin, normally low. |
| 5 | ØI | IN | Oscillator input. |
| 6 | ØO | OUT | Oscillator output. |
| 7 | RES | IN | Reset input, active high. Normally, pulled down to low level. |
| 8 | Xin | IN | Input (MT in) of microcassette signal from the CE-125 option. |
| 9 | ON | IN | ON (BREAK) key input, normally pulled down to low level. |
| 10 | Xout | OUT | Output (MT out 1) of microcassette signal to the CE-125 option and the buzzer. |
| 11 | Dis | OUT | LCD driver control signal. |
| 12 | HA | OUT | LCD driver clock, low during standby and in 2 kHz oscillation during display. |

| Pin No. | Signal name | IN/OUT | Description (Standby = power off) |
|---|---|---|---|
| 13 | iA8 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 14 | iA7 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 15 | iA6 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 16 | iA5 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 17 | iA4 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 18 | iA3 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 19 | iA2 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 20 | iA1 | IN/OUT | Key input/strobe signal, low during standby and key-in pulse is generated when low. |
| 21 | iB8 | IN | ACK signal that enables the CPU to read data through I/O port (PCU). |
| 22 | iB7 | IN | Data in (Din). Serial data input from PCU (bit by bit serial handshake). |
| 23 | iB6 | OUT | SEL2 output, P-type open drain. |
| 24 | iB5 | OUT | SEL1 output, P-type open drain. |
| 25 | iB4 | IN | Slide switch input. |
| 26 | iB3 | OUT | Key strobe output, low during standby and key-in pulse is generated when low. |
| 27 | iB2 | OUT | Key strobe output, low during standby and key-in pulse is generated when low. |
| 28 | iB1 | OUT | Key strobe output, low during standby and key-in pulse is generated when low. |
| 29 | VM | IN | LCD power supply. |
| 30 | VA | IN | LCD power supply. |
| 31 | GND | IN | Power supply. |
| 32 | H1 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 33 | H2 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 34 | H3 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 35 | H4 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 36 | H5 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 37 | H6 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 38 | H7 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 39 | H8 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 40 | H9 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 41 | H10 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 42 | H11 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 43 | H12 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 44 | H13 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 45 | H14 | OUT | LCD backplate signal, high impedance during standby and 4-level pulse during display. |
| 46 | H15 | — | Not used. (Display of this unit operates in 1/14 duty.) |
| 47 | H16 | — | Not used. (Display of this unit operates in 1/14 duty.) |
| 48 | $V_B$ | IN | LCD power supply, high during standby and low when the high level clock stops. |
| 49 | $V_{DiS}$ | IN | LCD power supply, high during standby and low when the high level clock stops. |
| 50 | $V_{CC}$ | IN | LCD power supply, normally low. |

| Pin No. | Signal name | IN/OUT | Description (Standby = power off) |
|---|---|---|---|
| 51 | $V_{DC}$ | OUT | LCD power supply, high during standby and low when the high level clock stops. |
| 52 | $V_{GG}$ | IN | Power supply normally low. |
| 53 | O8 | IN/OUT | Data bus, normally high impedance. |
| 54 | O7 | IN/OUT | Data bus, normally high impedance. |
| 55 | O6 | IN/OUT | Data bus, normally high impedance. |
| 56 | O5 | IN/OUT | Data bus, normally high impedance. |
| 57 | O4 | IN/OUT | Data bus, normally high impedance. |
| 58 | O3 | IN/OUT | Data bus, normally high impedance. |
| 59 | O2 | IN/OUT | Data bus, normally high impedance. |
| 60 | O1 | IN/OUT | Data bus, normally high impedance. |
| 61 | Fo5 | OUT | External system ROM chip enable (CE1). |
| 62 | Fo4 | OUT | Expansion RAM (PC-1251 RAM) chip enable (CE2). |
| 63 | Fo3 | OUT | Basic RAM (PC-1250, PC-1251) chip enable (CE3). |
| 64 | Fo2 | OUT | Data out (Dout), data output port to peripheral. |
| 65 | Fo1 | OUT | BUSH I/F output port output. |
| 66 | Bo8 | OUT | LCD driver LSI chip enable (CE4). |
| 67 | Bo7 | OUT | A14. Address bus, high during standby. |
| 68 | Bo6 | OUT | A13. Address bus, high during standby. |
| 69 | Bo5 | OUT | A12. Address bus, high during standby. |
| 70 | Bo4 | OUT | A11. Address bus, high during standby. |
| 71 | Bo3 | OUT | A10. Address bus, high during standby. |
| 72 | Bo2 | OUT | A9. Address bus, high during standby. |
| 73 | Bo1 | OUT | A8. Address bus, high during standby. |
| 74 | Ao8 | OUT | A7. Address bus, high during standby. |
| 75 | Ao7 | OUT | A6. Address bus, high during standby. |
| 76 | Ao6 | OUT | A5. Address bus, high during standby. |
| 77 | Ao5 | OUT | A4. Address bus, high during standby. |
| 78 | Ao4 | OUT | A3. Address bus, high during standby. |
| 79 | Ao3 | OUT | A2. Address bus, high during standby. |
| 80 | Ao2 | OUT | A1. Address bus, high during standby. |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

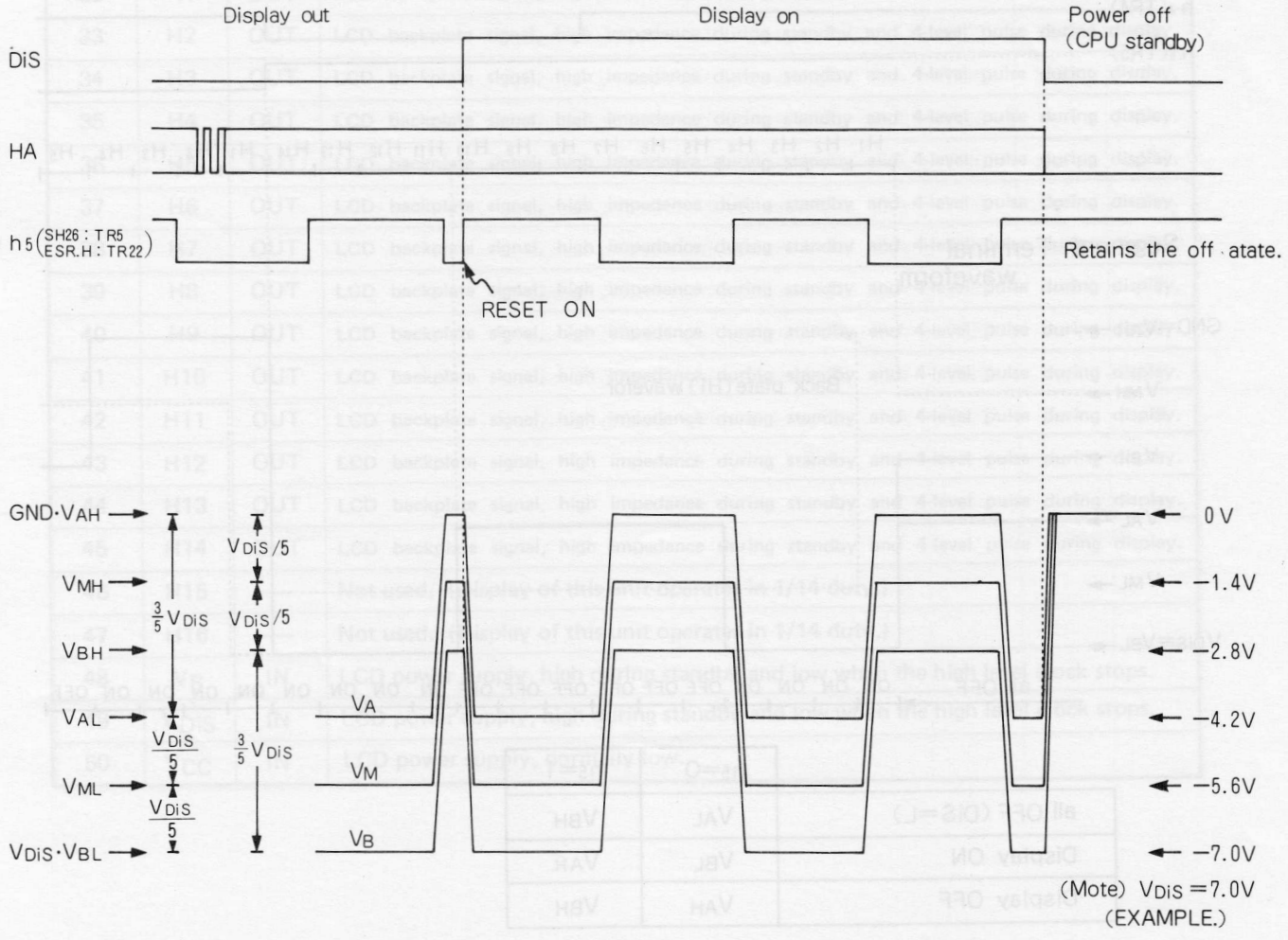
# 5. LCD DRiVE CiRCUiT AND TiMiNGS

## • LCD Driver LSi (SC43536)

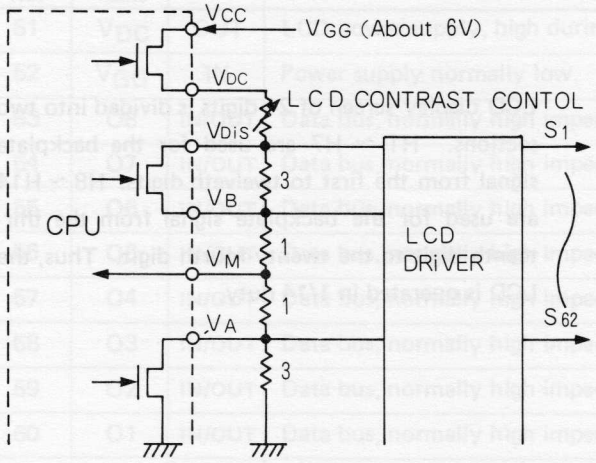



LCD display screen of 24 digits is divided into two sections. H1 ~ H7 are used for the backplate signal from the first to twelveth digits. H8 ~ H14 are used for the backplate signal from the thirteenth digit to the twenty-fourth digit. Thus, the LCD is operated in 1/14 duty.

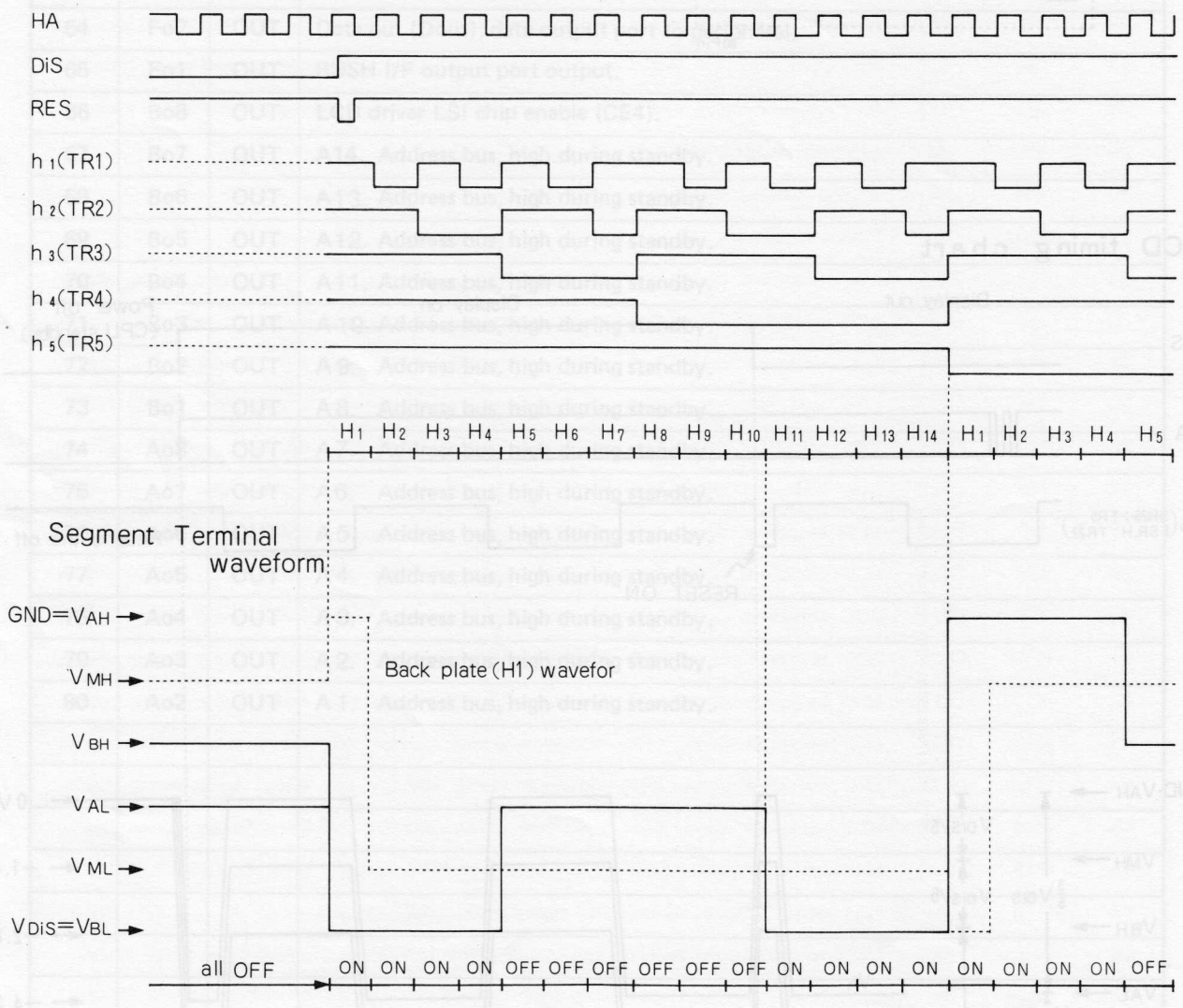
## • LCD timing chart



## • LCD POWER SUPPLY




## • COUNTER SECTiSN & Segment terminal waveform

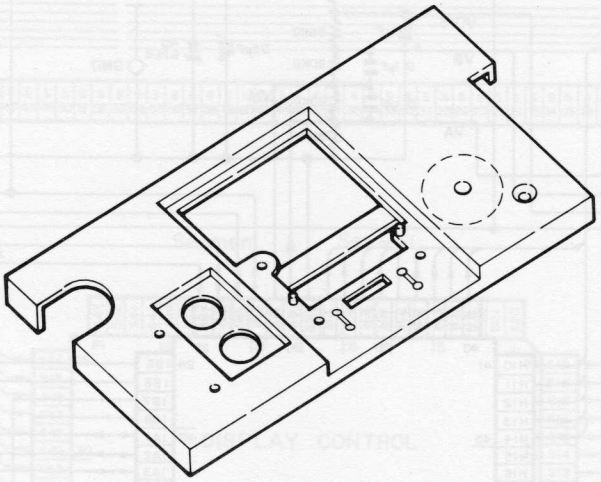



| | h5=0 | h5=1 |
|---|---|---|
| all OFF (DiS=L) | VAL | VBH |
| Display ON | VBL | VAH |
| Display OFF | VAH | VBH |

# 6. SERVICE PRECAUTIONS

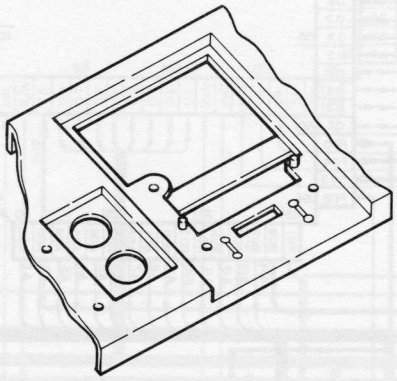
1. Since it is difficult to troubleshoot the main PWB because of chassis mounted on top of it, it is suggested that you use the service tool chassis (LCHSS1134CCZZ) which is smaller in size. Install this chassis for trouble-shooting purposes only. When unit is repaired, replace with original chassis.

2. When the memory module PWB is replaced it could be installed slightly out of alignment due to the play in the screw holes. Since this could lead to improper operation, replace the PWB again and press the ALL RESET switch befor resuming operation.

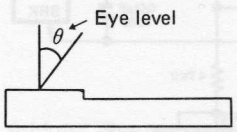


3. If the lithum battery is not installed properly and with good electrical contact problems such as flickering display or damage to other parts could result. Be sure the battery is properly installed.

4. Consumption current measurement
   - Supply voltage: 5.8 V
   - Consumption current:
     400 $\mu$A max. when ON (after pushing of the ON key).
     45 $\mu$A max. when OFF (after pushing of the OFF key).
     Be sure to press the ALL RESET switch before the measurement.



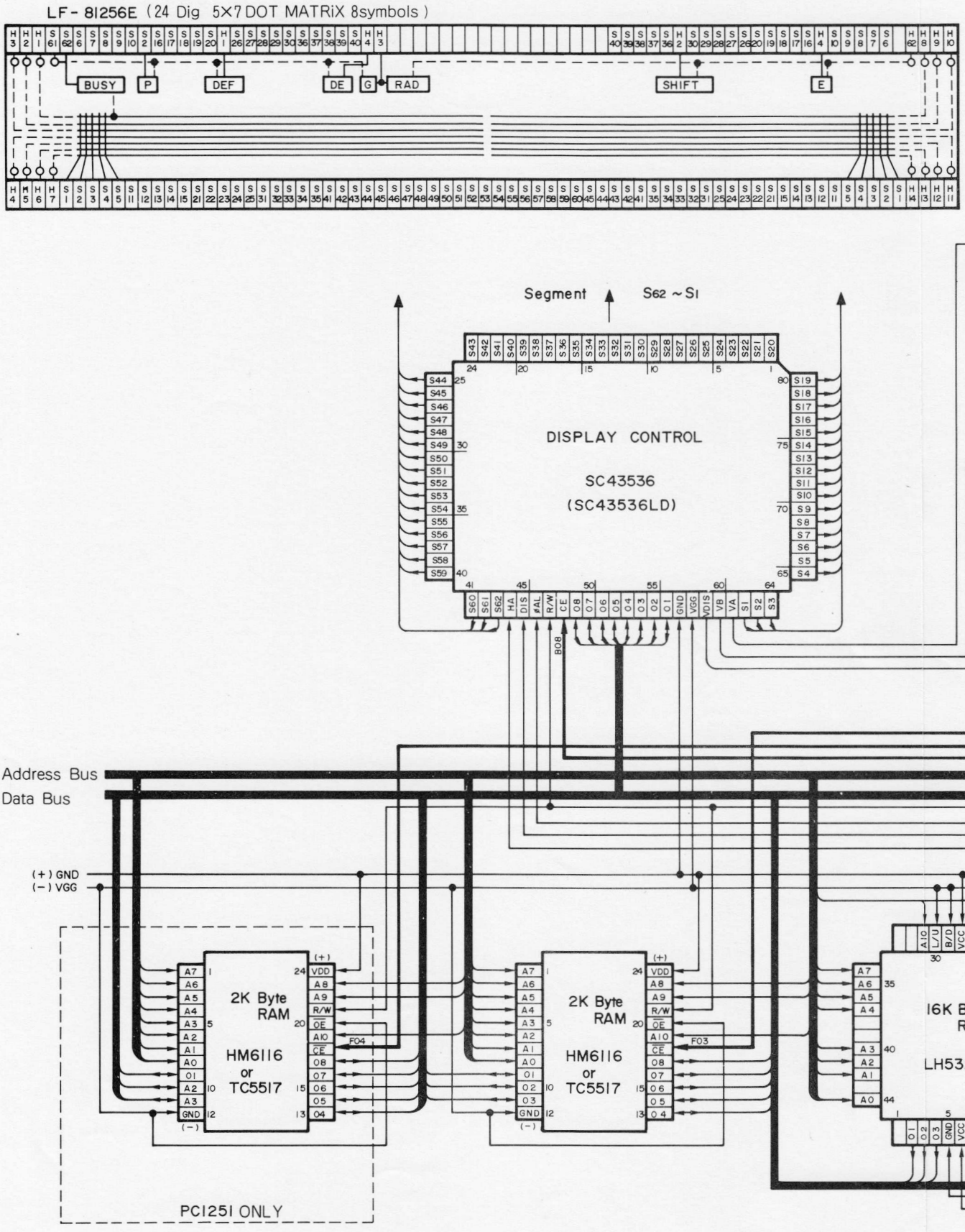
5. Checking display quality and adjusting potentio-meter.

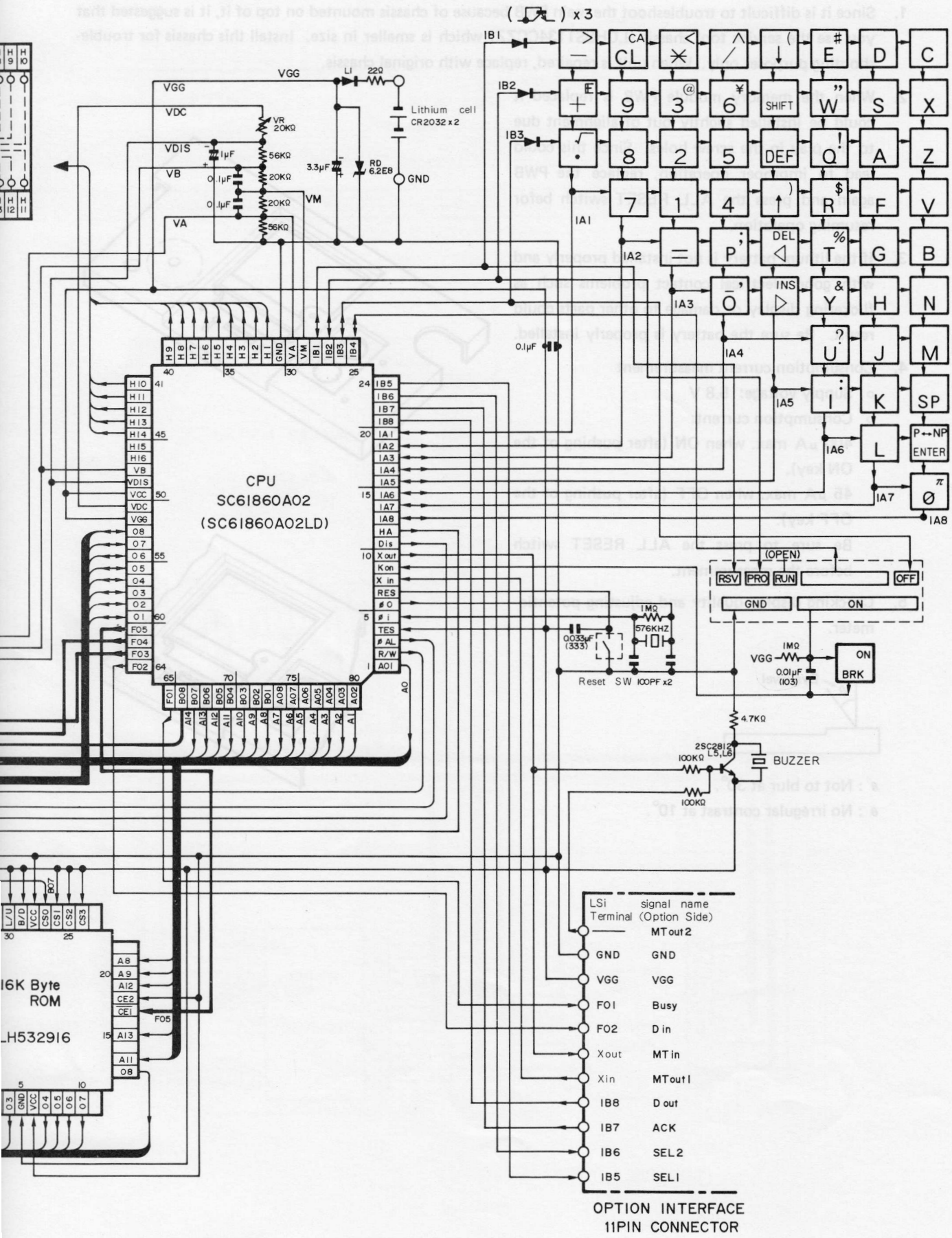



$\theta$ : Not to blur at 30°.

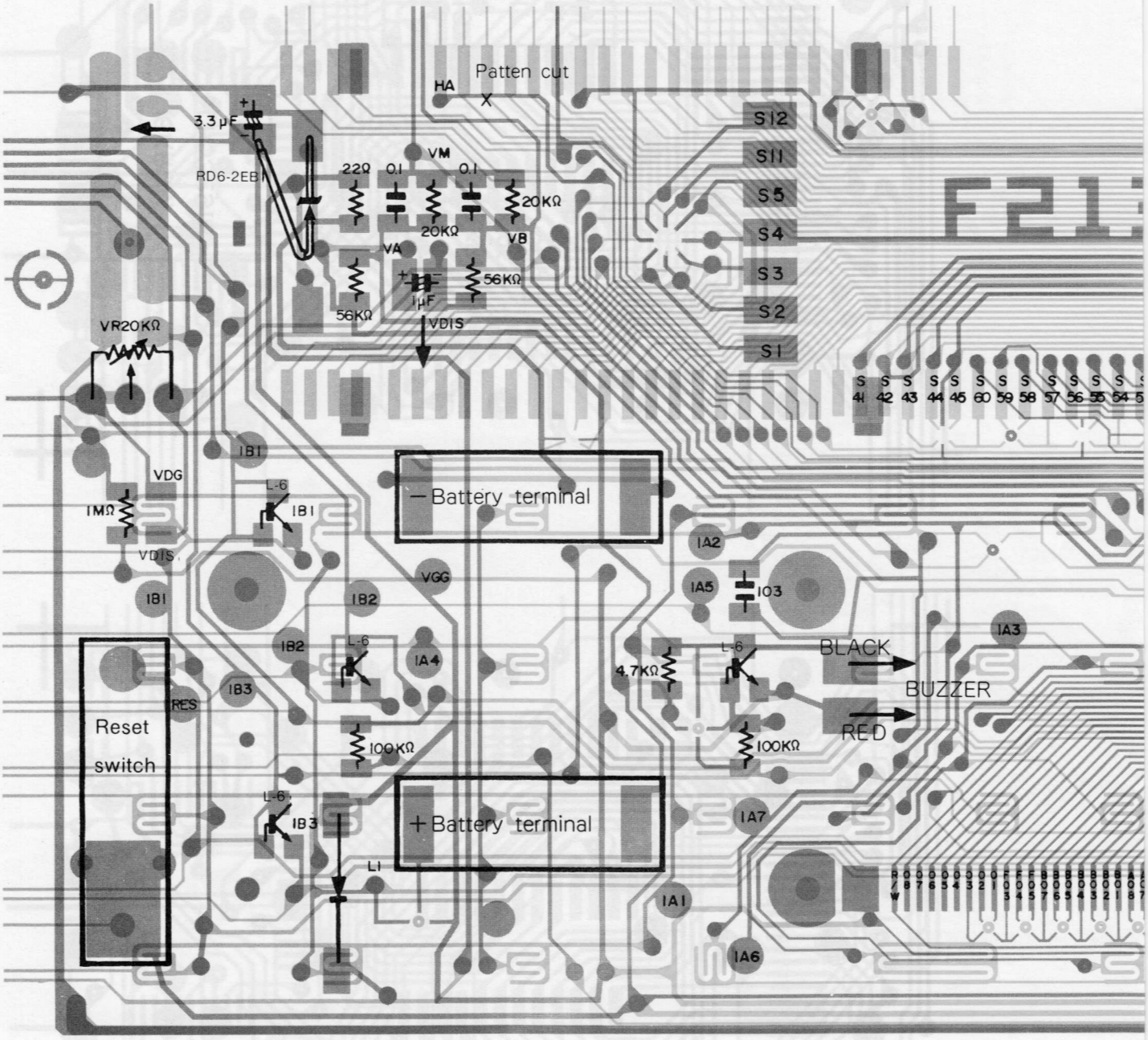
$\theta$ : No irregular contrast at 10°.

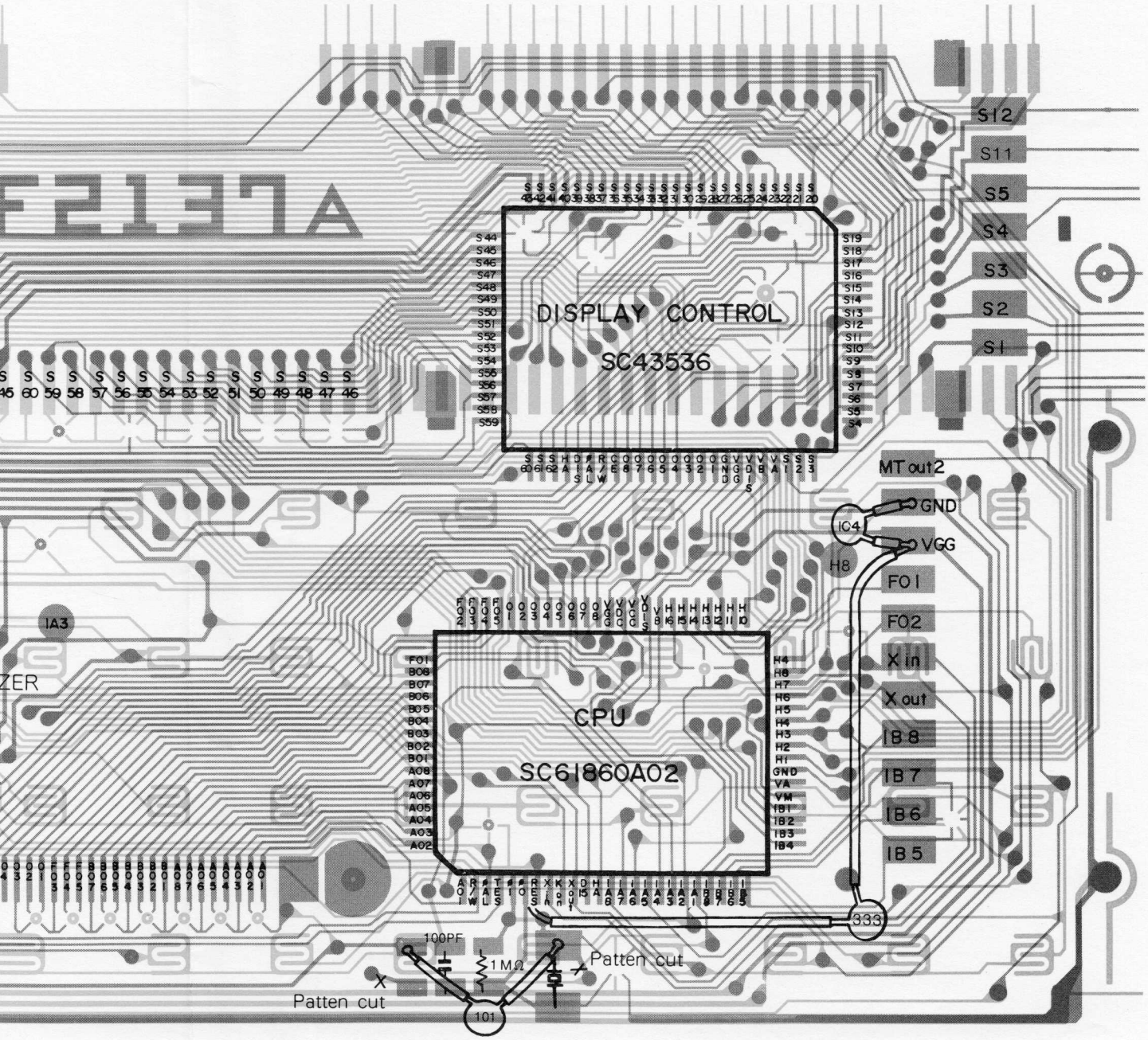
# 7. CiRCUiT DiAGRAM

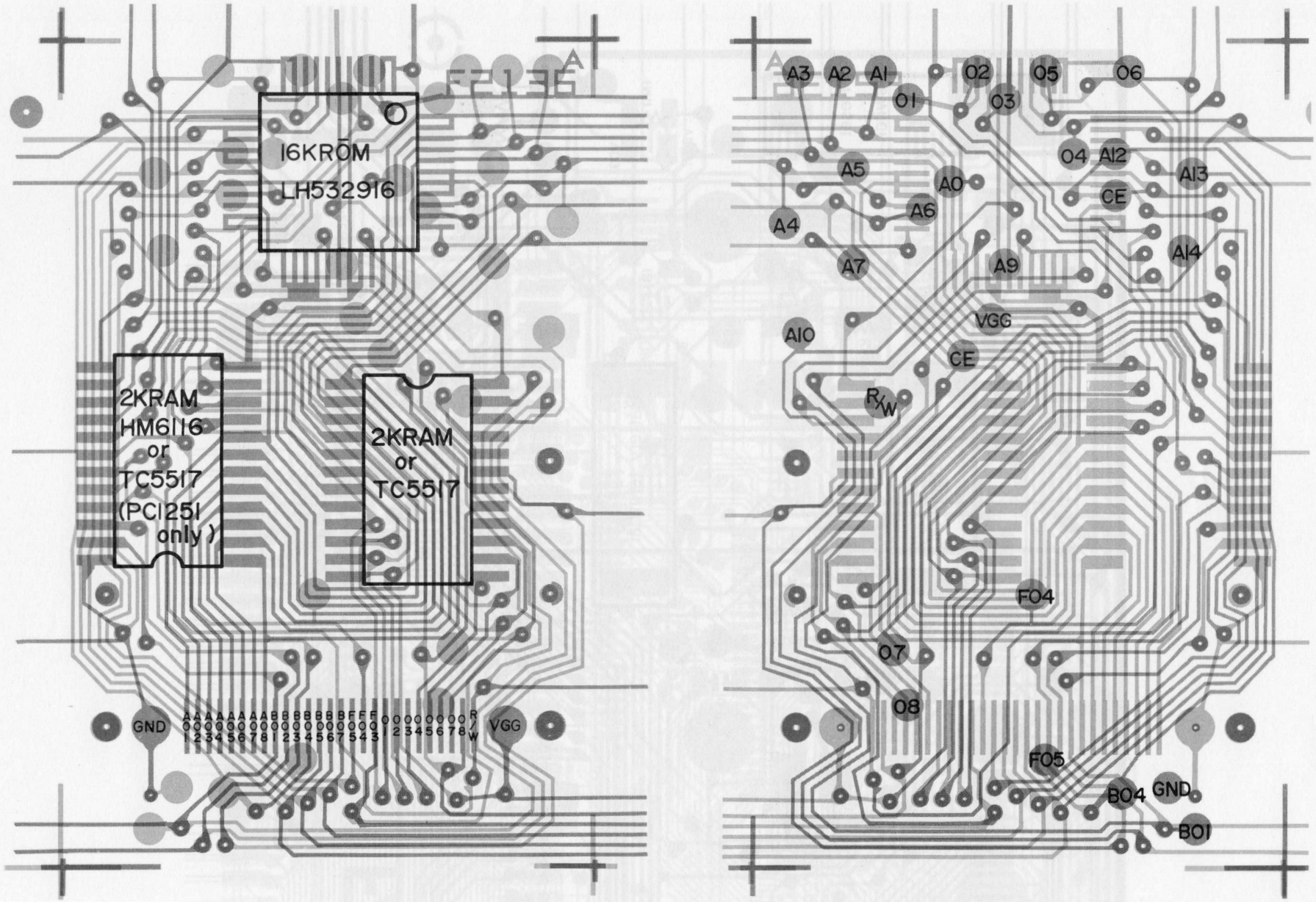


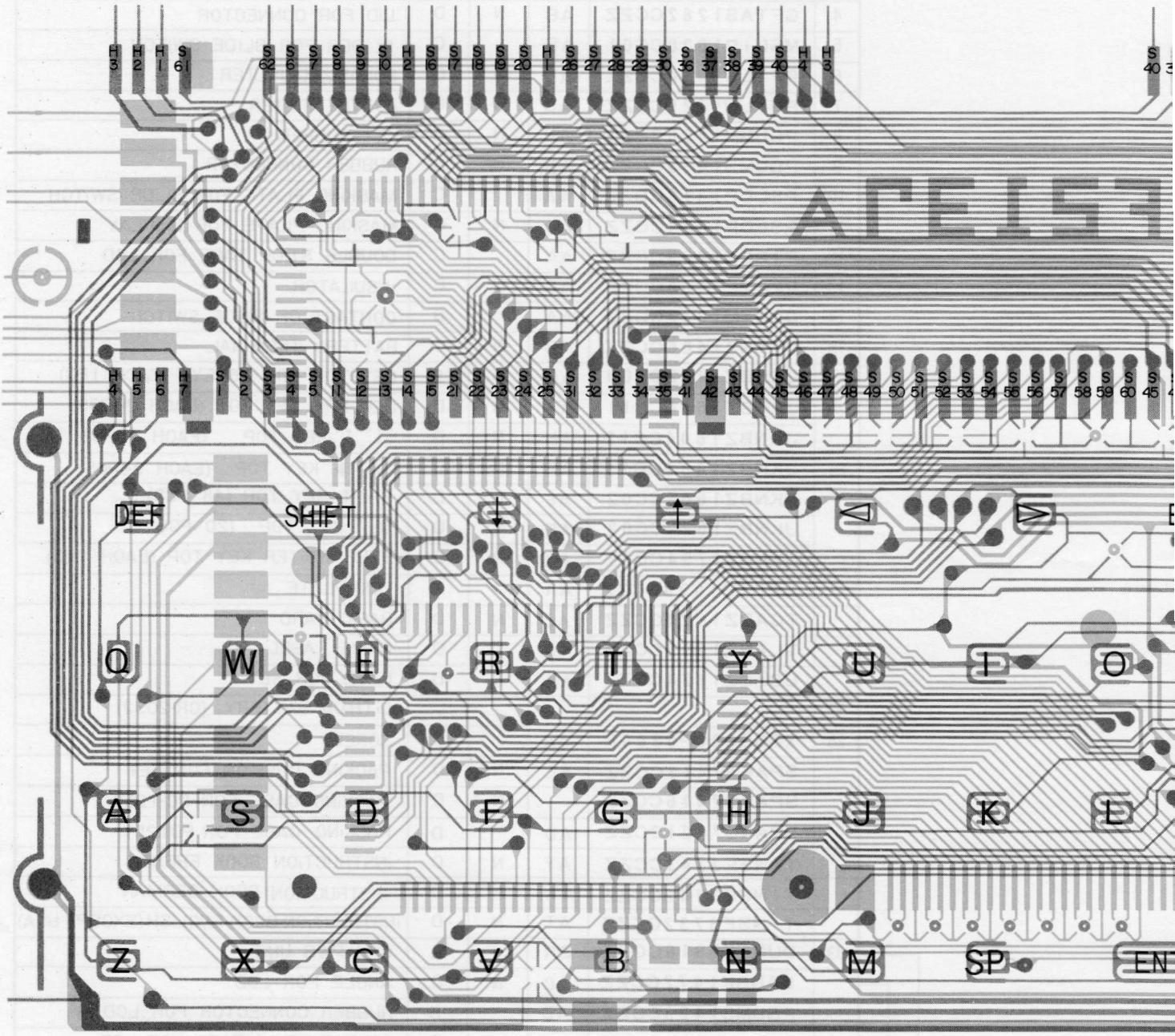

( ) x3
VGG
LI
220
Lithium cell
CR2032 x2
VDC
VR
20KΩ
VDIS
1μF
56KΩ
VB
0.1μF
20KΩ
VM
0.1μF
20KΩ
VA
56KΩ
3.3μF
RD
6.2E8
GND
IB1
IB2
IB3
IA1
IA2
IA3
IA4
IA5
IA6
IA7
IA8
0.1μF
CPU
SC61860A02
(SC61860A02LD)
H9 H8 H7 H6 H5 H4 H3 H2 H1 GND VA VM IB1 IB2 IB3 IB4
H10 H11 H12 H13 H14 H15 H16 VB VDIS VCC VDC VGG O8 O7 O6 O5 O4 O3 O2 O1 FO5 FO4 FO3 FO2
IB5 IB6 IB7 IB8 IA1 IA2 IA3 IA4 IA5 IA6 IA7 IA8 HA Dis Xout Kon X in RES ø0 ø i TES ø AL R/W AO1
FO1 BO8 BO7 BO6 BO5 BO4 BO3 BO2 BO1 AO8 AO7 AO6 AO5 AO4 AO3 AO2
AI4 AI3 AI2 AI1 AI0 A9 A8 A7 A6 A5 A4 A3 A2 A1
A0
CA CL
E
SHIFT
W
DEF
Q
DEL
R
T
INS
Y
U
I
P
L
P↔NP
ENTER
π
Ø
(OPEN)
RSV PRO RUN OFF
GND ON
1MΩ
576KHZ
0.033μF
(333)
Reset SW
100PF x2
VGG
1MΩ
0.01μF
(103)
ON
BRK
4.7KΩ
2SC2812
L5, L6
100KΩ
BUZZER
100KΩ
B07
L/U B/D VCC CS0 CS1 CS2 CS3
A8 A9 AI2 CE2 CE1 AI3 AI1 O8
O3 GND VCC O4 O5 O6 O7
FO5
16K Byte
ROM
LH532916
LSi Terminal
signal name (Option Side)
MTout2
GND GND
VGG VGG
FO1 Busy
FO2 Din
Xout MTin
Xin MTout1
IB8 Dout
IB7 ACK
IB6 SEL2
IB5 SEL1
OPTION INTERFACE
11PIN CONNECTOR

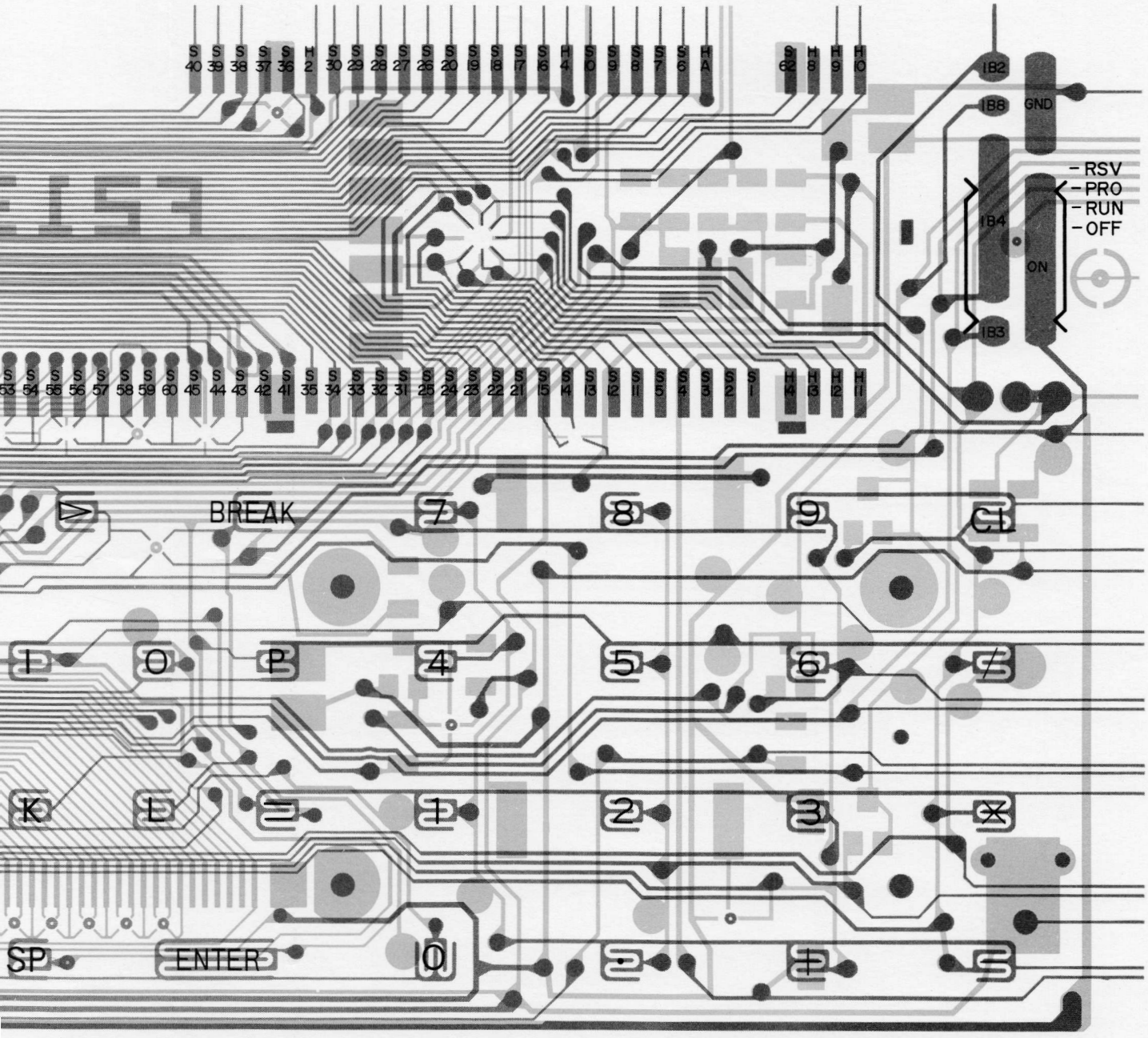
# 8. PARTS & SiGNAL POSiTiON




DISPLAY CONTROL
SC43536
CPU
SC61860A02
S12
S11
S5
S4
S3
S2
S1
MT out2
GND
VGG
IO4
H8
F01
F02
X in
X out
IB 8
IB 7
IB 6
IB 5
333
100PF
1 MΩ
Patten cut
Patten cut
101
IA3

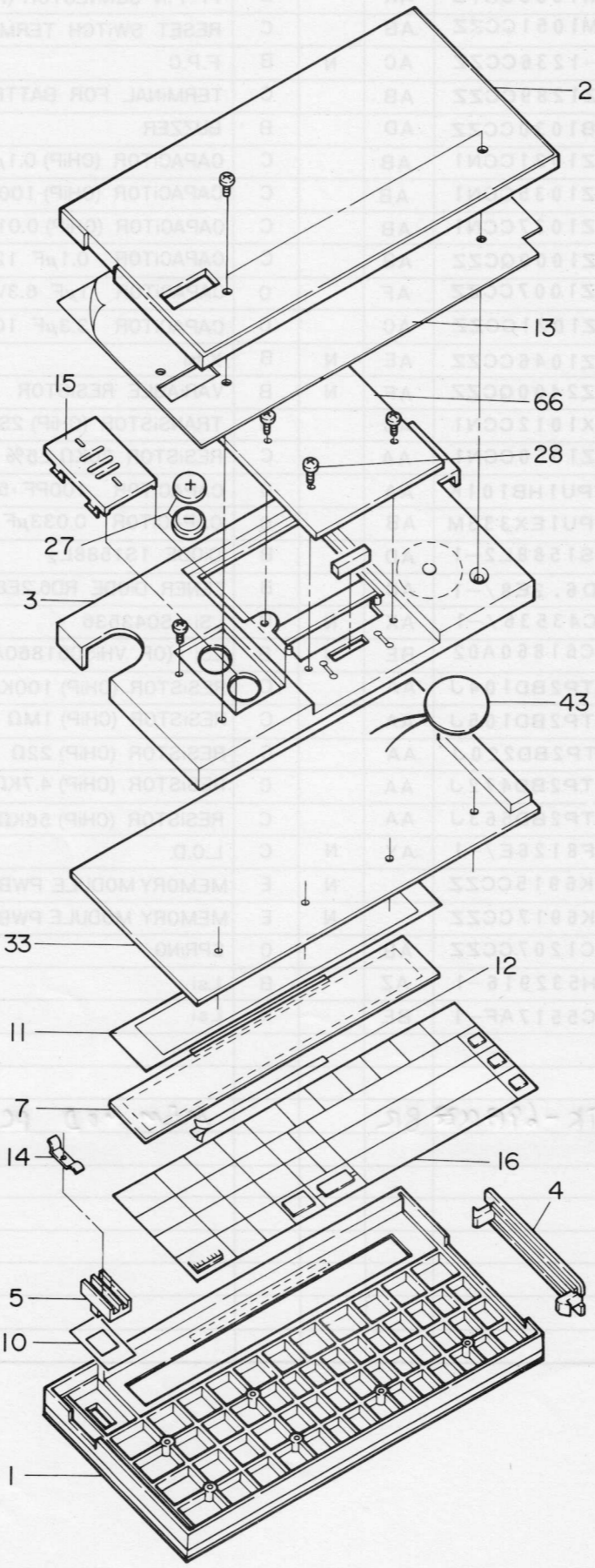

16KROM
LH532916
2KRAM
HM6116
or
TC5517
(PC1251
only)
2KRAM
or
TC5517
GND
VGG
R/W
A3
A2
A1
A0
A4
A5
A6
A7
A9
A10
A11
A12
A13
A14
CE
VGG
R/W
O1
O2
O3
O4
O5
O6
O7
O8
F04
F05
B04
B01
GND


DEF
SHIFT
Q
W
E
R
T
Y
U
I
O
A
S
D
F
G
H
J
K
L
Z
X
C
V
B
N
M
SP
EN


S 40 S 39 S 38 S 37 S 36 H 2 S 30 S 29 S 28 S 27 S 26 S 20 S 19 S 18 S 17 S 16 H 4 S 10 S 9 S 8 S 7 S 6 H A S 62 H 8 H 9 H 10
IB2
IB8
GND
IB4
IB3
ON
- RSV
- PRO
- RUN
- OFF
S 53 S 54 S 55 S 56 S 57 S 58 S 59 S 60 S 45 S 44 S 43 S 42 S 41 S 35 S 34 S 33 S 32 S 31 S 25 S 24 S 23 S 22 S 21 S 15 S 14 S 13 S 12 S 11 S 5 S 4 S 3 S 2 S 1 H 14 H 13 H 12 H 11
BREAK
7
8
9
CL
I
O
P
4
5
6
K
L
1
2
3
SP
ENTER
0

| No. | PARTS CODE | PRiCE RANK | N E W MARK | PARTS RANK | PARTS NEME |
|---|---|---|---|---|---|
| | QCNCW1306CC1B | AK | | B | 11 PiN CONNECTOR (F) |
| | QCNTM1051CCZZ | AB | | C | RESET SWiTCH TERMiNAL |
| 43 | QCNW-1236CCZZ | AC | N | B | F.P.C |
| | QTANZ1289CCZZ | AB | | C | TERMiNAL FOR BATTERY |
| | RALMB1030CCZZ | AD | | B | BUZZER |
| | RC-CZ1021CCN1 | AB | | C | CAPACiTOR (CHiP) 0.1μF |
| | RC-CZ1035CCN1 | AB | | C | CAPACiTOR (CHiP) 100PE |
| | RC-CZ1037CCN1 | AB | | C | CAPACiTOR (CHiP) 0.01μF |
| | RC-CZ1000QCZZ | AB | | C | CAPACiTOR 0.1μF 12V |
| | RC-SZ1007CCZZ | AF | | C | CAPACiTOR 1μF 6.3V |
| | RC-SZ1021CCZZ | AC | | C | CAPACiTOR 3.3μF 10V |
| | RCRSZ1046CCZZ | AE | N | B | X'tal |
| | RVR-Z2400QCZZ | AF | N | B | VARiABLE RESiSTOR |
| | RH-iX1012CCN1 | AC | | B | TRANSiSTOR (CHiP) 2SC2812 (L5,L6) |
| | RR-KZ1050CCN1 | AA | | C | RESiSTOR 20KΩ±5% |
| | VCKYPU1HB101K | AA | | C | CAPACiTOR 100PF 50V |
| | VCTYPU1EX333M | AB | | C | CAPACiTOR 0.033μF 25V |
| | VHDDS1588L2-1 | AD | | B | DiODE 1S1588L2 |
| | VHERD6.2E8/-1 | AC | | B | ZENER DiODE RD6.2E8 |
| | VHiSC43536/-1 | AX | N | B | LSi SC43536 |
| | VHiSC61860A02 | BE | N | B | LSi (OR VHiSC61860A01) |
| | VRS-TP2BD104J | AA | | C | RESiSTOR (CHiP) 100KΩ |
| | VRS-TP2BD105J | AA | | C | RESiSTOR (CHiP) 1MΩ |
| | VRS-TP2BD220J | AA | | C | RESiSTOR (CHiP) 22Ω |
| | VRS-TP2BD472J | AA | | C | RESiSTOR (CHiP) 4.7KΩ |
| | VRS-TP2BD563J | AA | | C | RESiSTOR (CHiP) 56KΩ |
| | VVLLF8126E/-1 | AY | N | C | L.C.D. |
| 66 | DUNTK6915CCZZ | | N | E | MEMORY MODULE PWB UNiT FOR PC1250 |
| | DUNTK6917CCZZ | | N | E | MEMORY MODULE PWB UNiT FOR PC1251 |
| | MSPRC1207CCZZ | AB | | C | SPRiNG |
| | VHiLH532916-1 | AZ | | B | Lsi |
| | VHiTC5517AF-1 | BE | | B | Lsi |
| | | | | | |
| | | | | | |
| 80 | DUNTK-6917CCZZ | BR | | | MEM MOD PC1250A |

• PARTS GUDE



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